

PCB STACK UP

LAYER 1 : TOP
LAYER 2 : GND1
LAYER 3 : IN1
LAYER 4 : VCC
LAYER 5 : IN2
LAYER 6 : IN3
LAYER 7 : GND2
LAYER 8 : BOT

TE4 Block Diagram

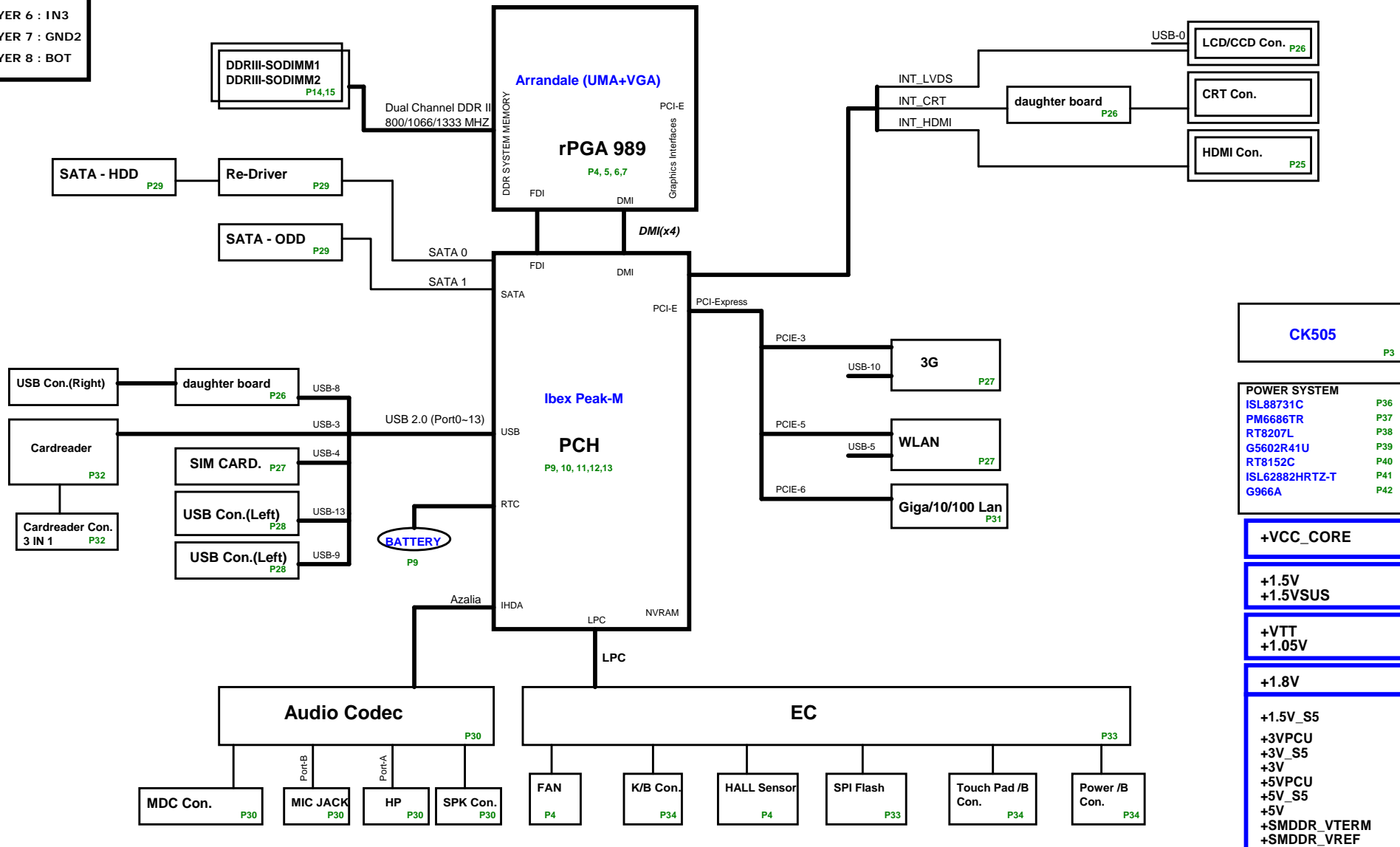







Table of Contents

[illegible]

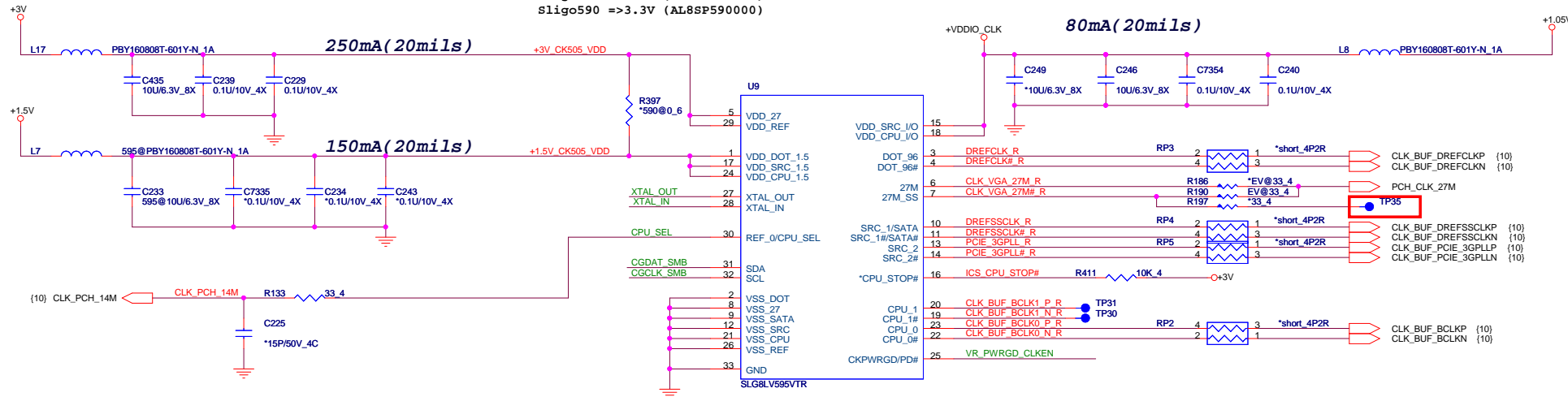
POWER PLANE	VOLTAGE	CONTROL SIGNAL	Power States ACTIVE IN
VIN	10V~+19V		S0-S5
+VCCRTC	+3.0V~+3.3V		S0-S5
+3V	+3.3V	MAIN_ON	S0
+3V_S5	+3.3V	S5_ON	S0-S5
+3V_HDP	+3.3V	MAIN_ON	S0
+3VPCU	+3.3V	AC/DC Insert enable	S0
+5V	+5V	MAIN_ON	S0
+5V_S5	+5V	S5_ON	S0-S5
+5VPCU	+5V	AC/DC Insert enable	S0-S5
WIMAX_P	+3.3V	WMAX_P for WLAN	
+1.8V	+1.8V	MAIN_ON	S0
+1.5V	+1.5V	MAIN_ON	S0
+1.5V_SUS	+1.5V	SUSON	S0-S3
+VCC_CORE		VRON	S0
+VTT	+1.05V	MAIN_ON	S0
+1.05V	+1.05V	MAIN_ON	S0
+VAXG		MPWROK	S0

GND PLANE	PAGE
 8769AGND	33
 Audio_GND	30
 Shield_GND	30
 GND	ALL
 ISL95870A_AGND	30

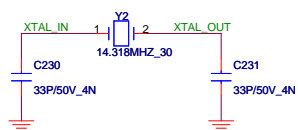
CLOCK Gen [CLK]

Pin1/17/24
 Sligo595 =>1.5V (AL000595000)
 Sligo590 =>3.3V (AL8SP590000)

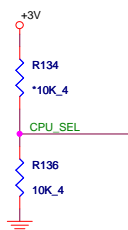
03



CLK CRYSTAL

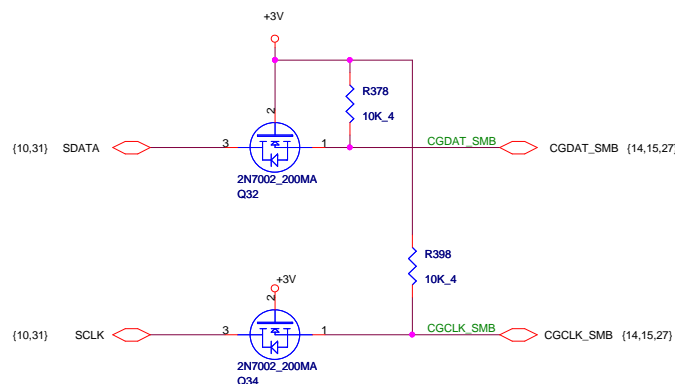


CLK CPU_SEL

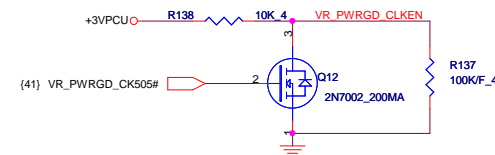


	0	1
CPU_SEL	CPU =133MHz (default)	CPU=100MHz

CLK I2C

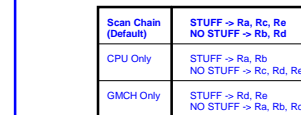
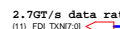


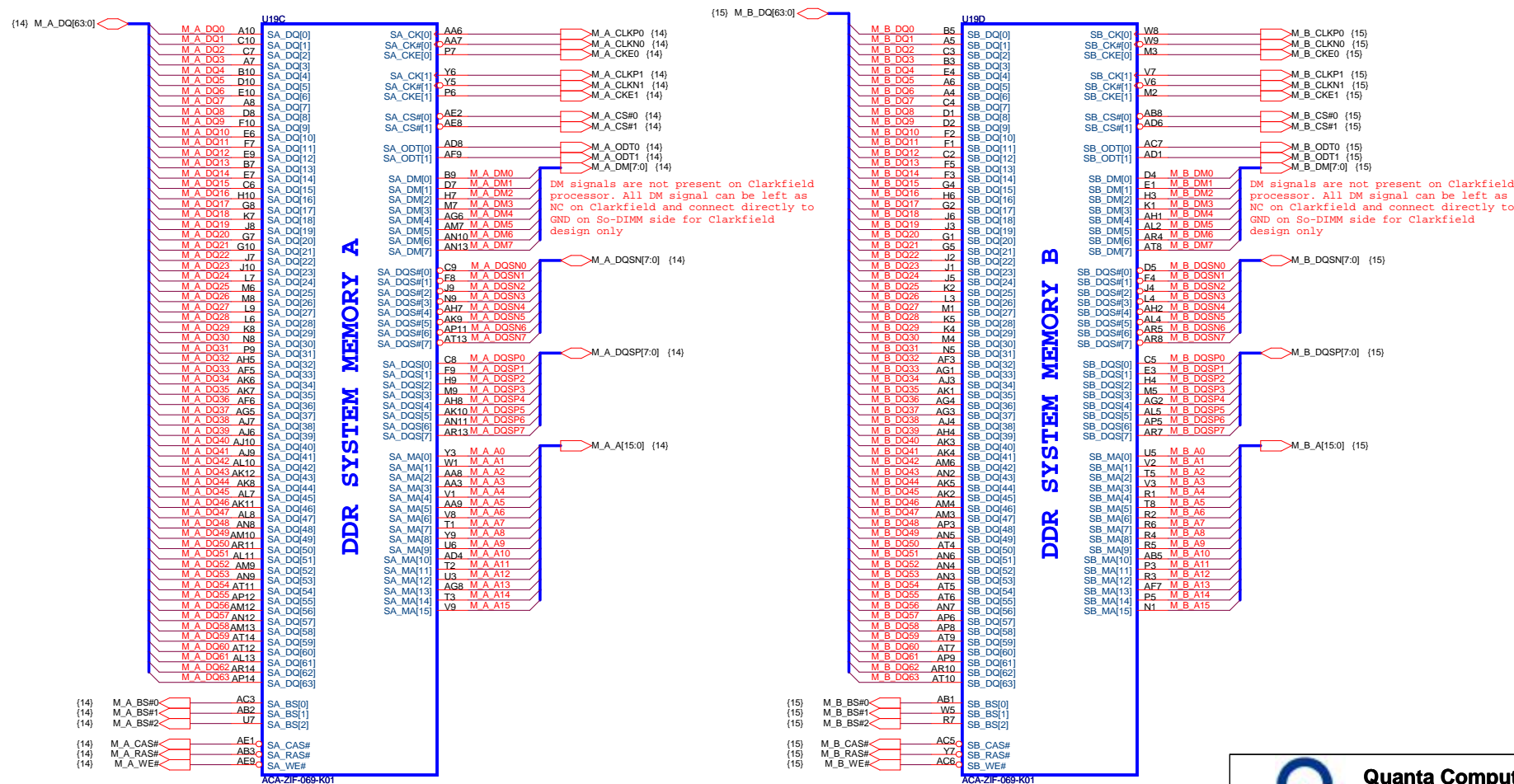
CLK POWERGOOD

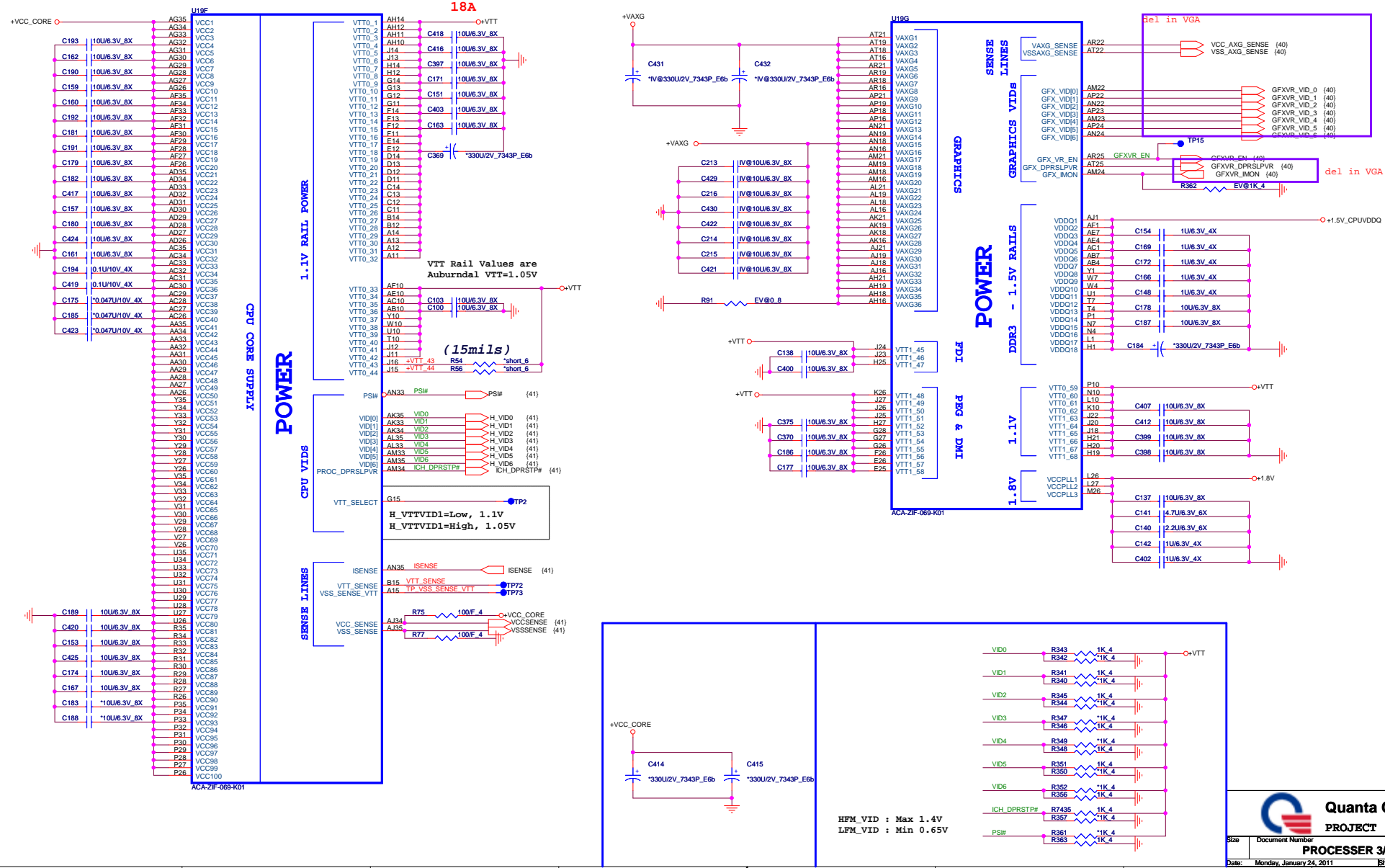


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	CLOCK GENERATOR	A1A
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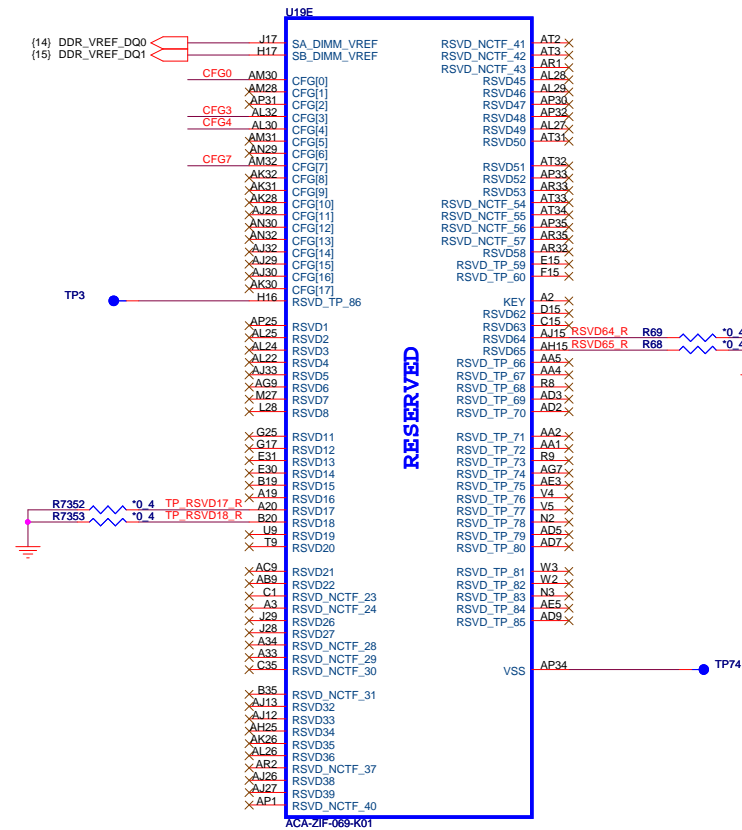
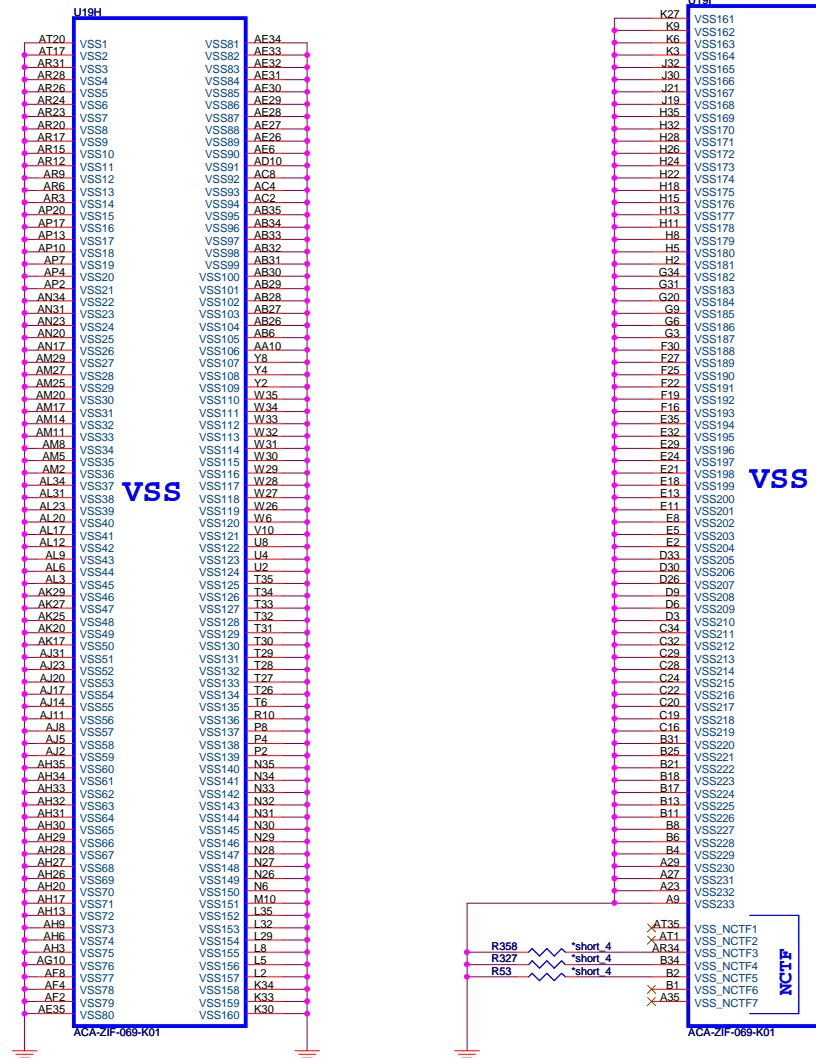






AUBURNDALE/CLARKSFIELD PROCESSOR (GND)

AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)

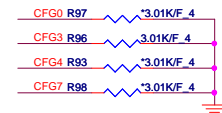


The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.

CFG[1:0] - PCI_Epress Configuration Select
 * 11= 1 x 16 PEG
 * 10= 2 x 8 PEG

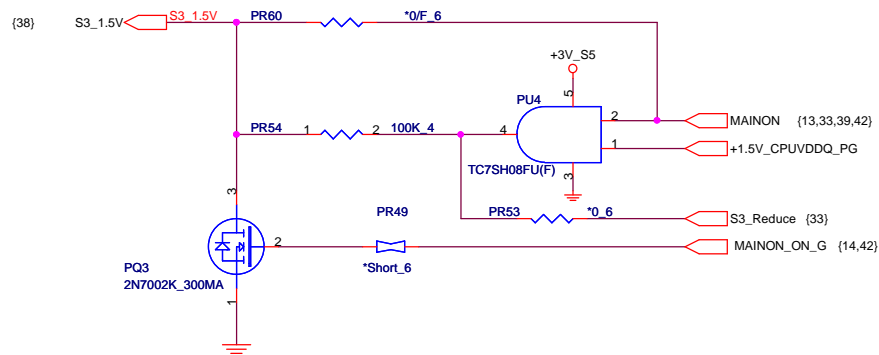
For Discrete only

	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed 15 -> 0, 14 -> 1

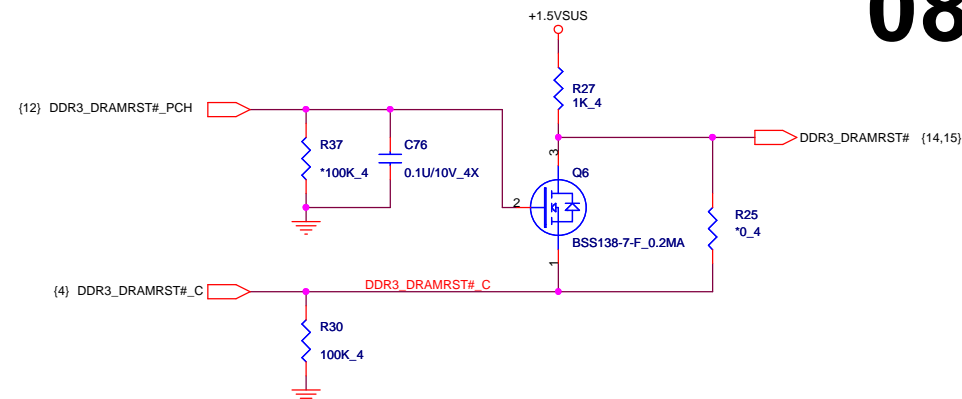


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PROCESSOR 4/4 (GND)
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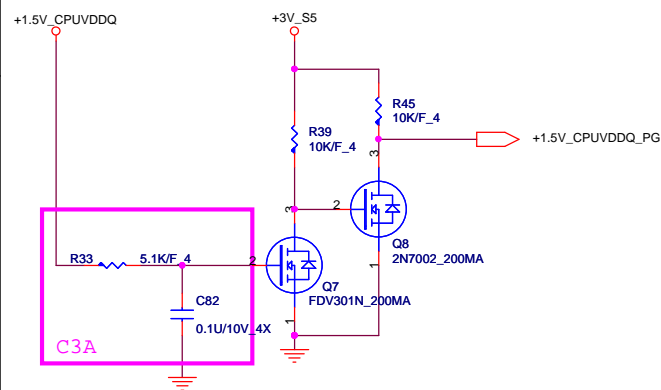


DRAM Reset

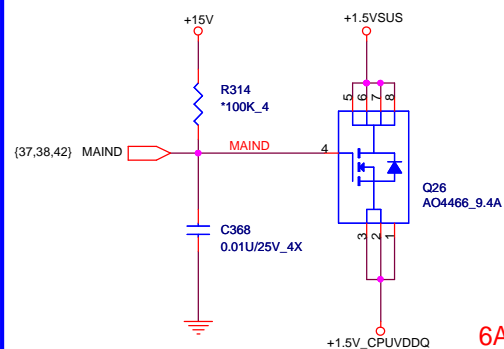


08

VDDQ Power Good



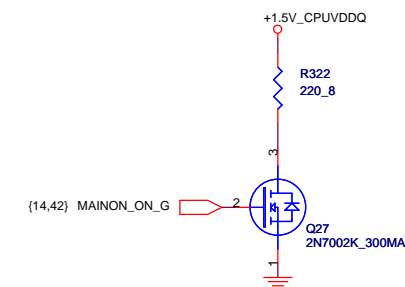
VDDQ Power Switch



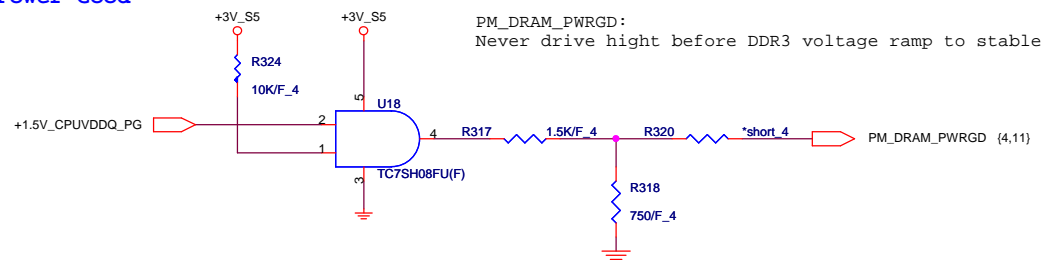
6A/maximum

Q7044可換A06402A, cost down.

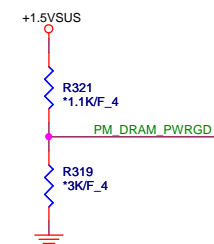
VDDQ Discharge



DRAM Power Good



PM_DRAM_PWRGD:
Never drive high before DDR3 voltage ramp to stable

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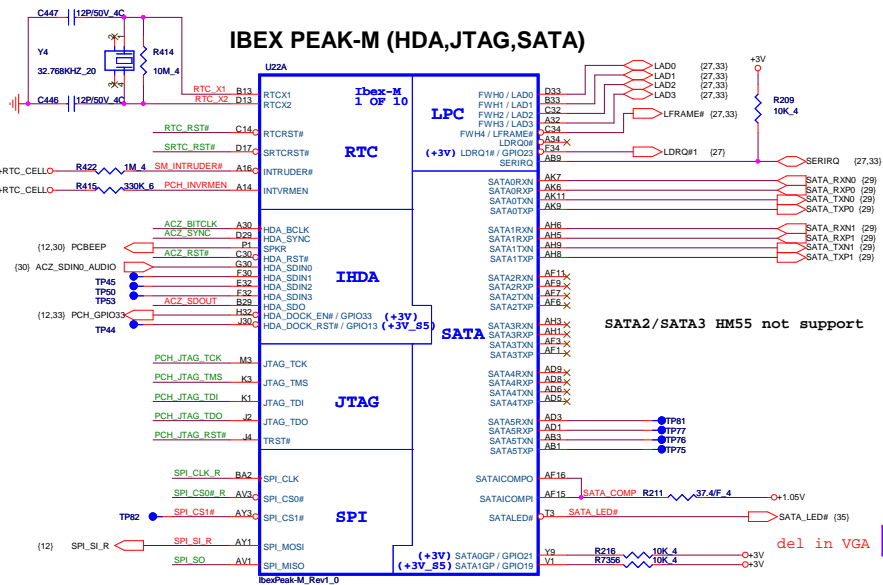
S3 Power Reduction

Rev
A1A

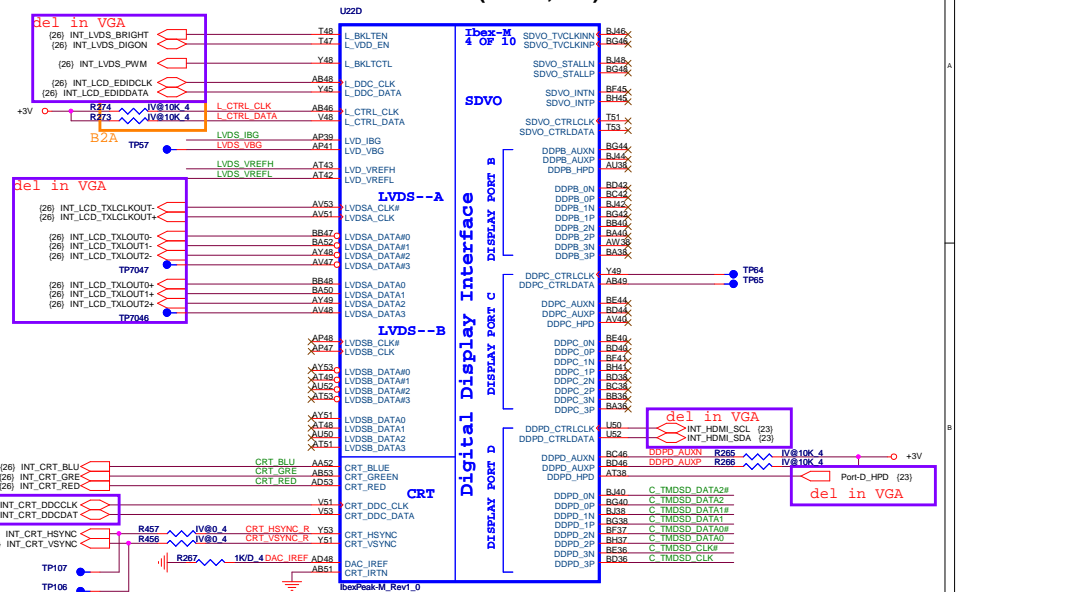
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INTVRMEN - Integrated SUS 1.1V VRM Enable
High - Enable Internal VRs

IBEX PEAK-M (HDA,JTAG,SATA)

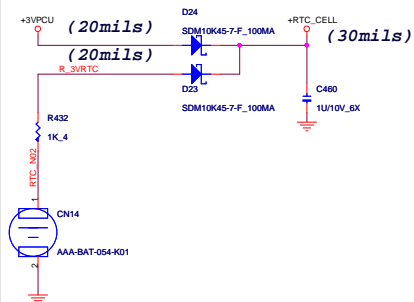


IBEX PEAK-M (LVDS,DDI)



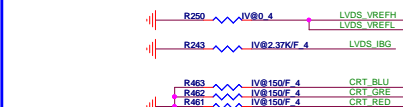
[RTC]

RTC BATTERY

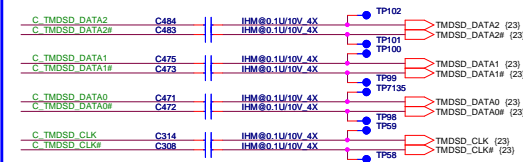


DDP Setting

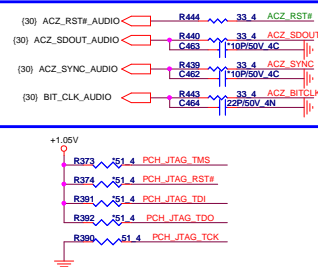
Port	Strap	How to enable Port?	How to disable Port?
LVDS	L_DDC_DATA	PU to 3.3V with 2.2k+/- 5%	NC
Port B	SDVO_CTRLDATA	PU to 3.3V with 2.2k+/- 5%	NC
Port C	DDPC_CTRLDATA	PU to 3.3V with 2.2k+/- 5%	NC
Port D	DDPD_CTRLDATA	PU to 3.3V with 2.2k+/- 5%	NC
eDP	CFG[4]	PD to GND directly	NC



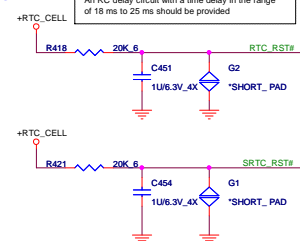
HDMI



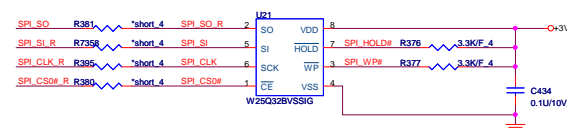
Alzia



RESET JUMP



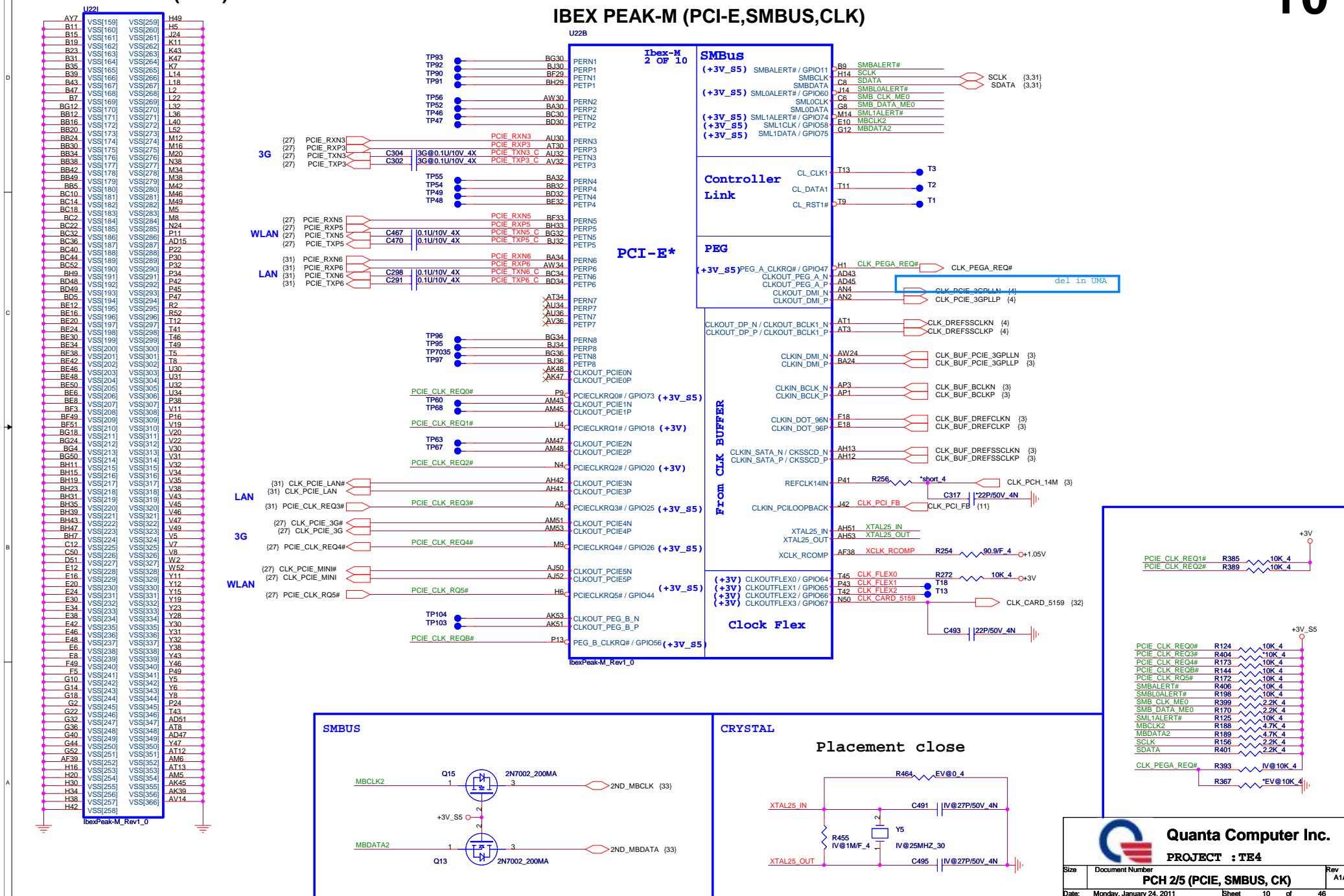
4M byte SPI ROM



PCH	2MB	4MB	8MB
PM55	●	●	●
HM55	●	●	●
HM57/PM57	●	●	●
QM57/QS57	●	●	●

IBEX PEAK-M (GND)

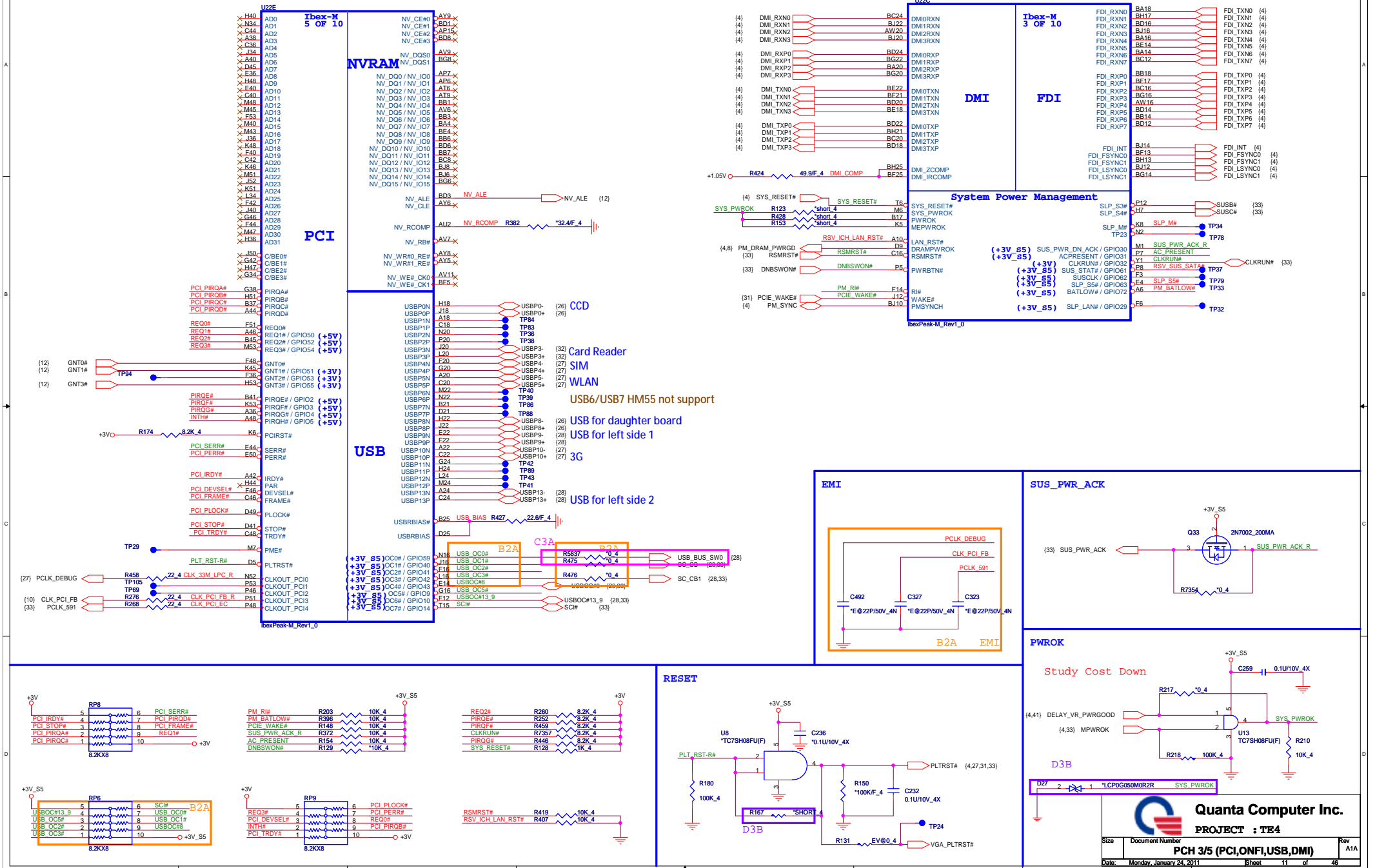
IBEX PEAK-M (PCI-E,SMBUS,CLK)



IBEX PEAK-M (PCI,USB,NVRAM)

IBEX PEAK-M (DMI,FDI,GPIO)

11



IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)

IBEX PEAK-M (GND)

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PCH Strap Pin Configuration Table

SPKR

(9,30) PCBEEP \rightarrow *1K/F_4 \rightarrow R388 \rightarrow +3V

0 = Default Mode (Internal weak Pull-down)
1 = No Reboot Mode with TCO Disabled

GNT3# / GPIO55

(11) GNT3# \rightarrow R460 \rightarrow *10K/F_4

0 = Default Mode (Internal weak Pull-down)
1 = No Reboot Mode with TCO Disabled

HDA_DOCK_EN #GPIO33

(9,33) PCH_GPIO33 \rightarrow R237 \rightarrow 1K/F_4 \rightarrow JP1 \rightarrow *SHORT PAD

0 = Top Block Swap Mode
1 = Default Mode (Internal pull-up)

GNT0#, GNT1#

(11) GNT0# \rightarrow R270 \rightarrow *1K/F_4
(11) GNT1# \rightarrow R271 \rightarrow *1K/F_4

Boot BIOS Strap		
PCH_GNT0#	GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

SPI_MOSI

(9) SPI_SI_R \rightarrow R7355 \rightarrow *1K_4 \rightarrow +3V

NV_ALE

(11) NV_ALE \rightarrow R403 \rightarrow *10K_4 \rightarrow +1.8V

1 = Enabled
0 = Disabled (Default)

GPIO8

GPIO8 \rightarrow R149 \rightarrow *10K_4 \rightarrow +3V_S5

This signal has a weak internal pull up.
NOTE: This signal should not be pulled low

GPIO15

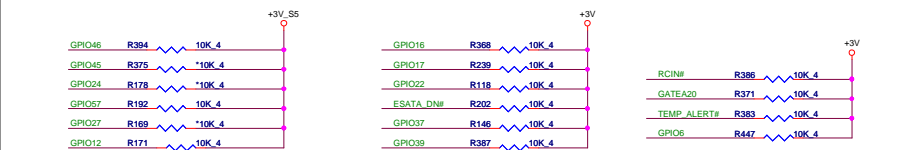
GPIO15 \rightarrow R128 \rightarrow *1K_4 \rightarrow +3V_S5

0 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality
1 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality

GPIO27

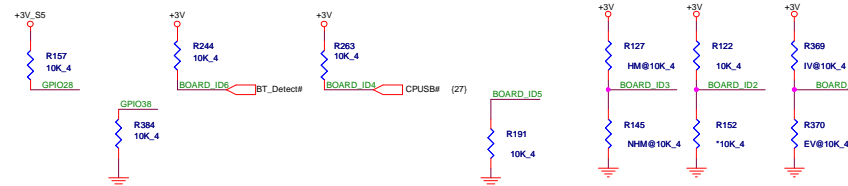
GPIO27 \rightarrow R182 \rightarrow *10K_4

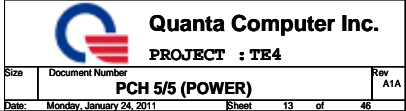
0 = Disables the VccVRRM. Need to use on-board filter circuits for analog rails.
1 = Enables the internal VccVRRM to have a clean supply for analog rails.
This signal has a weak internal pull-up.



BOARD ID SETTING

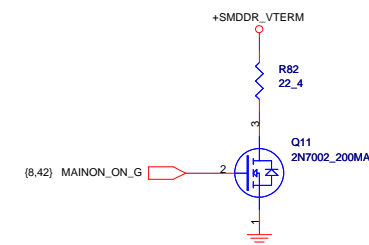
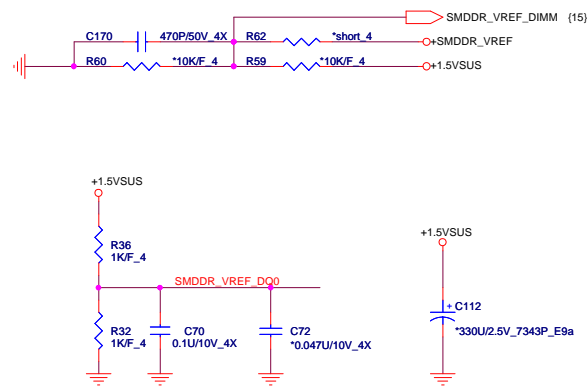
Board ID	ID1	ID2	ID3	ID4	ID5	ID6	GPIO28	GPIO38
UMA SKU	H							
VGA SKU	L							
W/ MDC		H						
W/O MDC		L						
W/ HDMT			H					
W/O HDMT			L					
W/O 3G				H				
W/ 3G				L				
15* 14*					H			
W/O BT						H		
W/ BT					L			
14 or 15 13							H	
Old HW(2010)								H
New HW(2011)								L



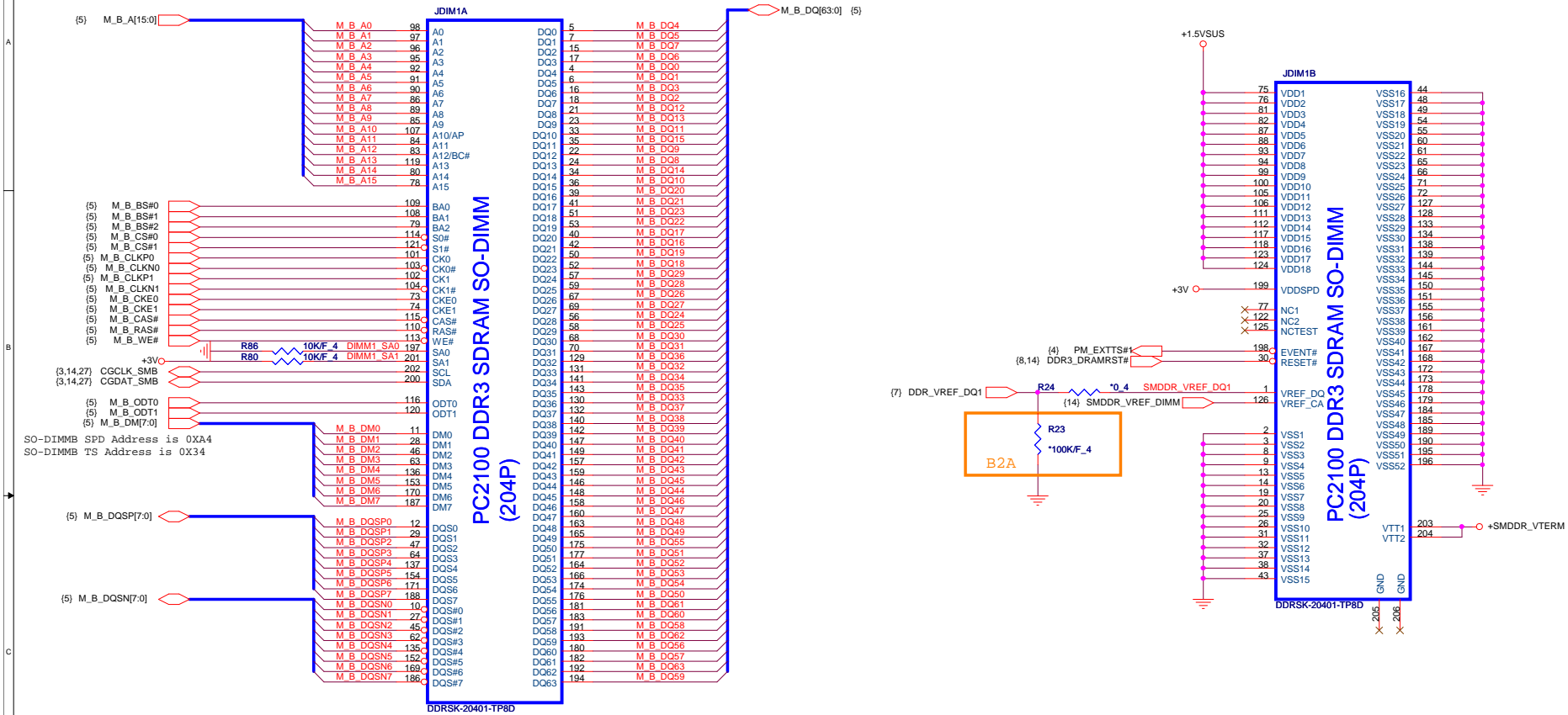




Some Projects replace 10UF 0805 by 4.7UF 0603
It can cost down 30%

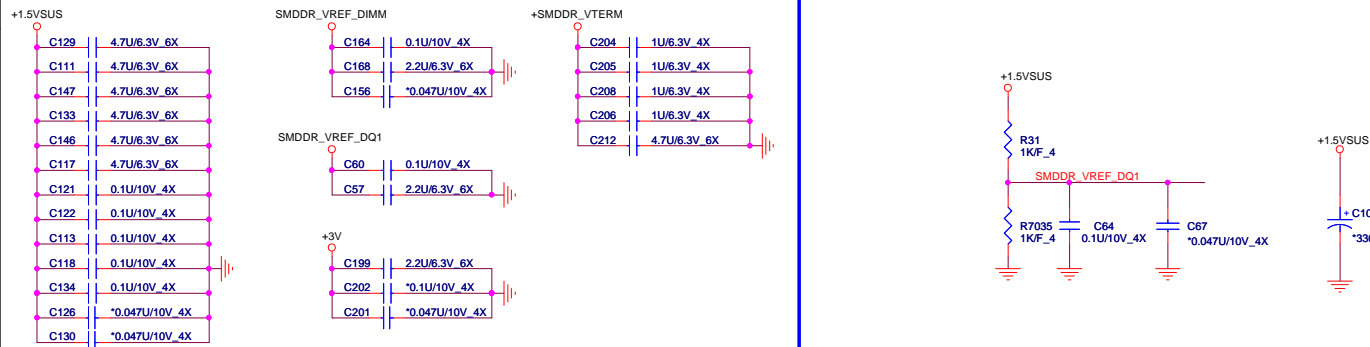


H=8



Place these Caps near So-Dimm1.

Some Projects replace 10UF 0805 by 4.7UF 0603
It can cost down 30%



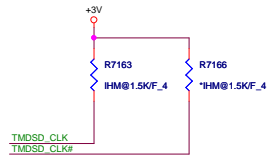
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DDR3 DIMM-1

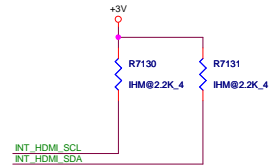
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	DDR3 DIMM-1	A1A
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Display Port Enable

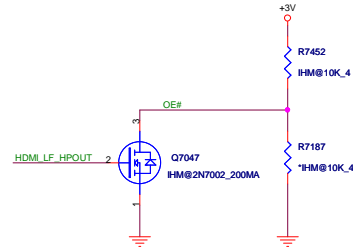
[HDM]



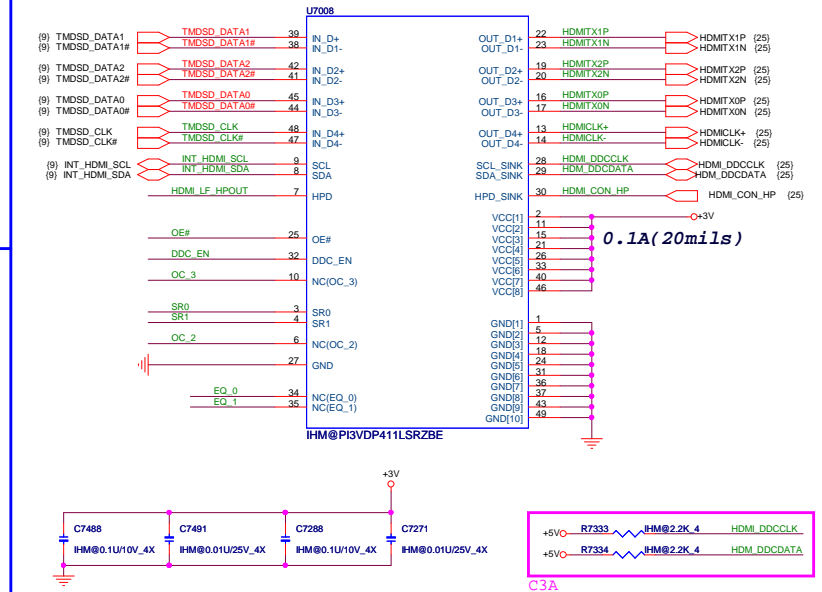
I2C PU



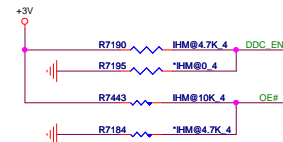
LEVEL SHIFT ENABLE



HDMI LEVEL SHIFT (UMA)



LEVEL SHIFT SETTING



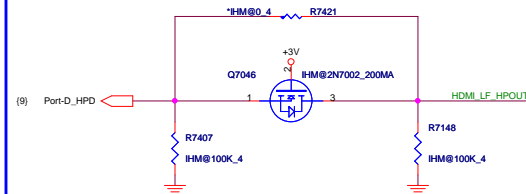
Slew Rate Control Function

SR1	SR0	Rise/Fall Time
1	1	140ps
1	0	130ps
0	1	120ps
0	0	110ps

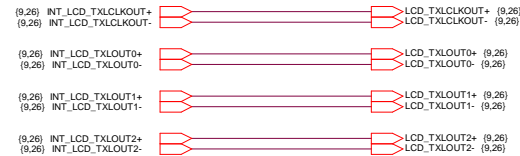
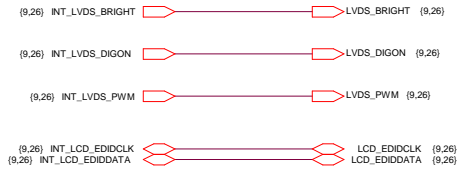
Reserve



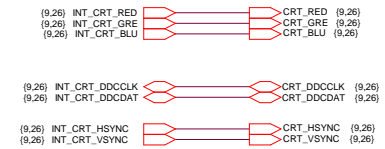
Hot Plug Detector (UMA)



LVDS (UMA)

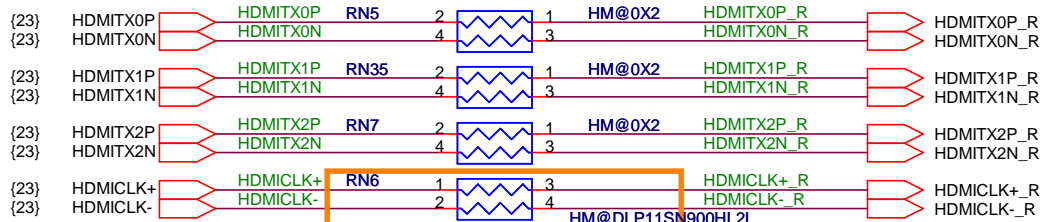
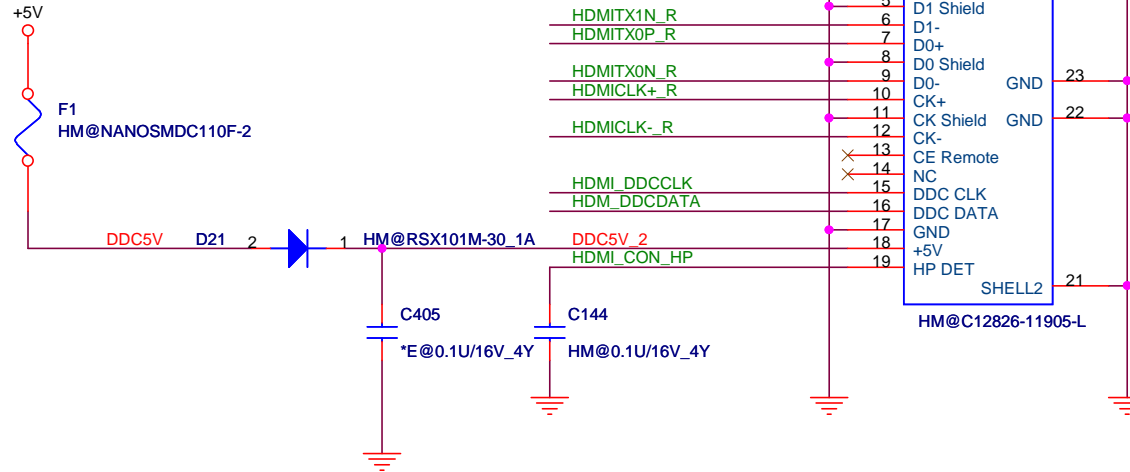


CRT (UMA)

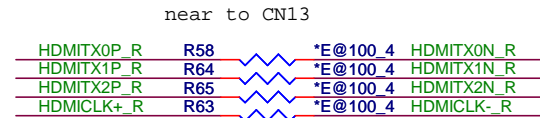
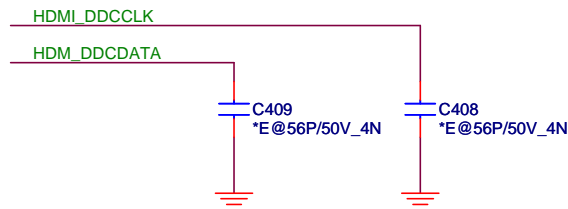


HDMI Conn [HDM]

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RI138: footprint is choke model
B2A




near to CN13

B2A

EMI

此組之後可以刪掉，重覆到了

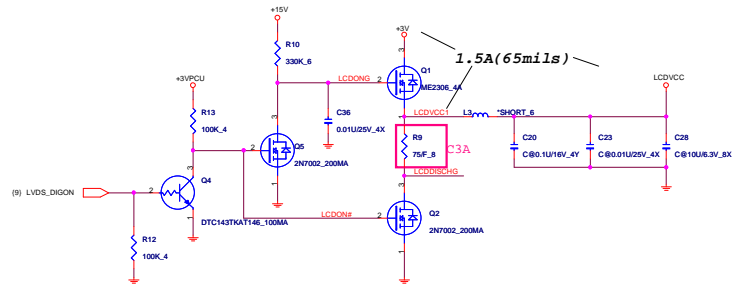


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	HDMI CONN	A1A
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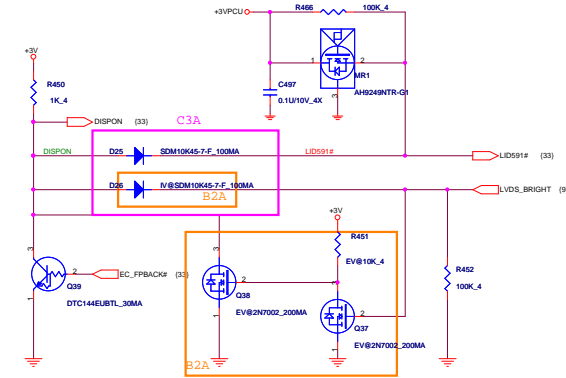
LCD POWER SWITCH

<LDS>



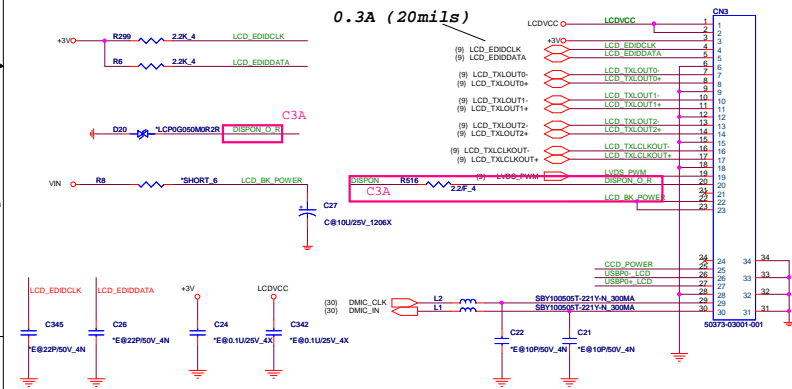
HALL Sensor

<HSR>



LCD Panel Module

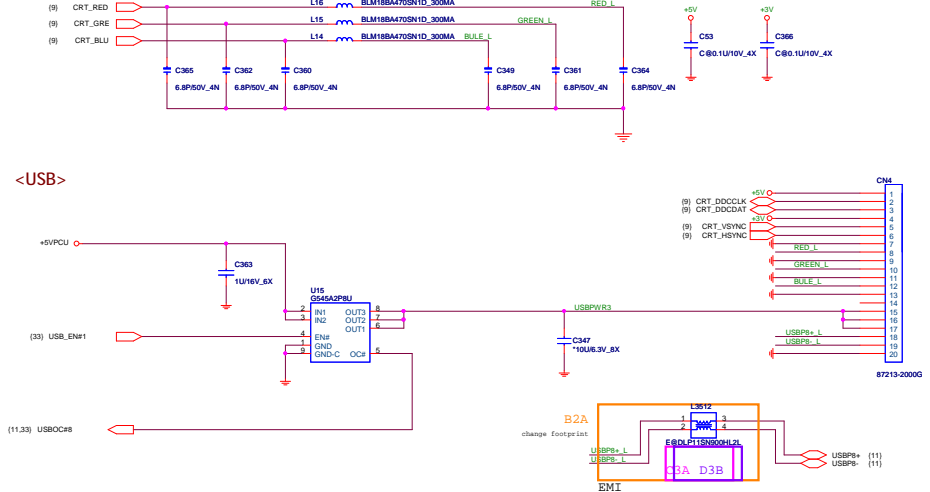
<LDS>



CRT

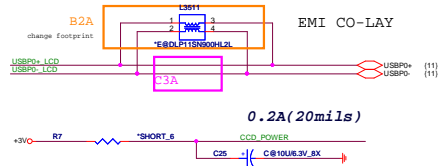
<CRT>

USB for CRT BOARD (Right) <USB>

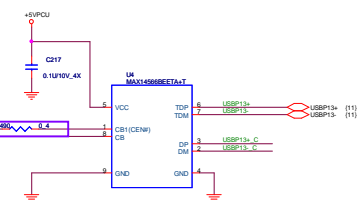


CCD

<CCD>



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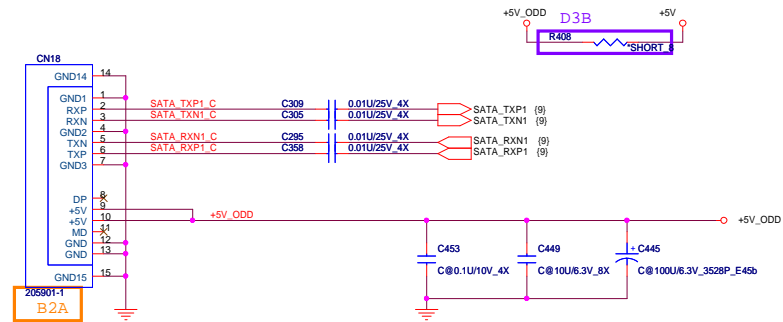


CB0	CB1	Status
0	0	Auto mode
0	1	Force dedicated charger mode
1	X	Pass-Through(USB) mode: Connect DP/DM to TDP/TDM

Figure 10 shows two circuit boards. The left board is a USB-to-RS485 module. It features a USB connector with pins 1 (USB D+), 2 (USB D-), 3 (USB GND), and 4 (USB VCC). The module includes a MAX3232CPE IC and a MAX485 IC. The MAX485 IC is configured with OE# and DE# pins. The RS485 connector has pins 1 (RS485 A), 2 (RS485 B), 3 (RS485 GND), and 4 (RS485 VCC). The right board is an RS485 module. It features an RS485 connector with pins 1 (RS485 A), 2 (RS485 B), 3 (RS485 GND), and 4 (RS485 VCC). The module includes a MAX485 IC. The RS485 transceiver ICs are configured with OE# and DE# pins. The RS485 transceiver ICs are configured with OE# and DE# pins. The RS485 transceiver ICs are configured with OE# and DE# pins.

SATA ODD

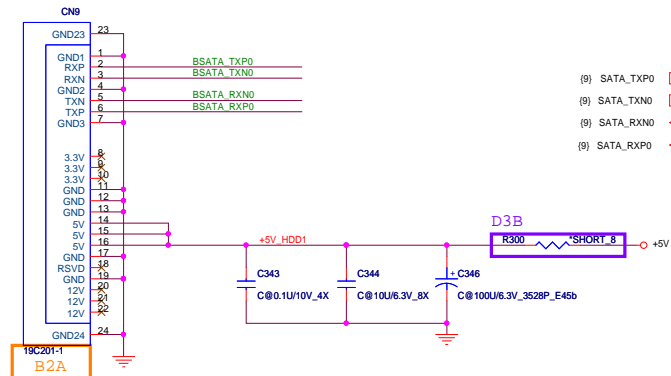
[ODD]



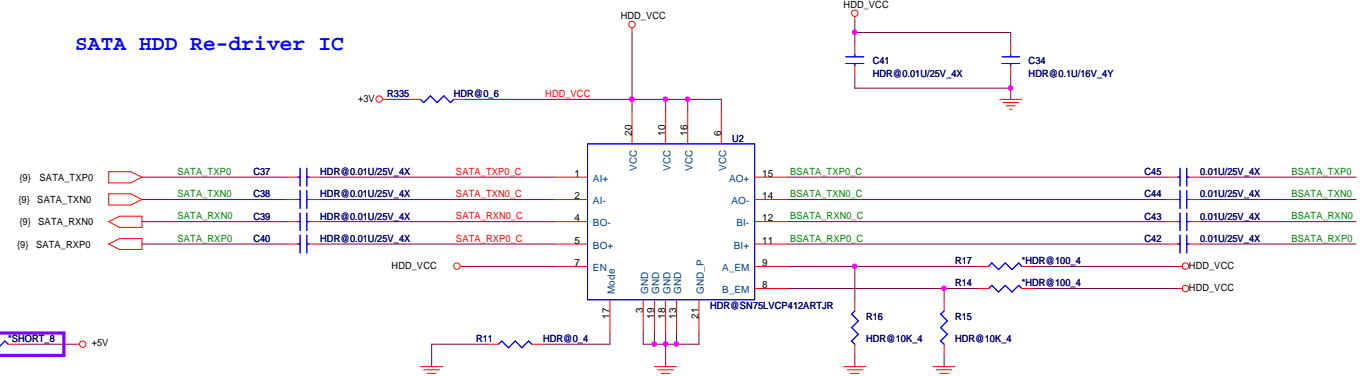
ODD Zero power . (Only for Intel) <OZP>

SATA HDD

[HDD]



SATA HDD Re-driver IC



SATA Re-driver Bypass

Colay with Redriver IC

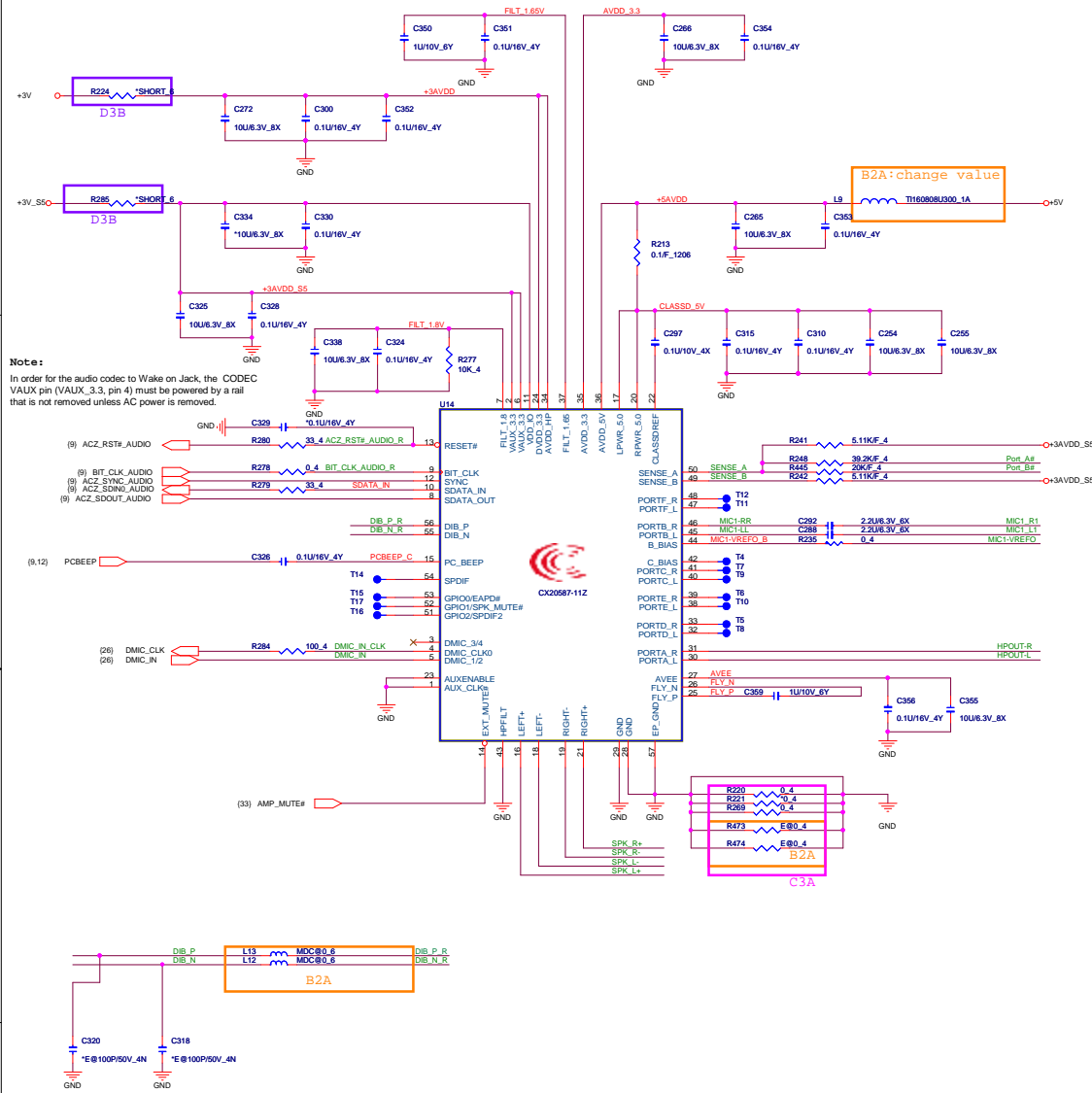
SATA_TXP0	R306	HDO@0.4	R302	HDO@0.4	BSATA_TXP0_C
SATA_TXN0	R305	HDO@0.4	R303	HDO@0.4	BSATA_TXN0_C
SATA_RXN0	R309	HDO@0.4	R304	HDO@0.4	BSATA_RXN0_C
SATA_RXP0	R308	HDO@0.4	R307	HDO@0.4	BSATA_RXP0_C

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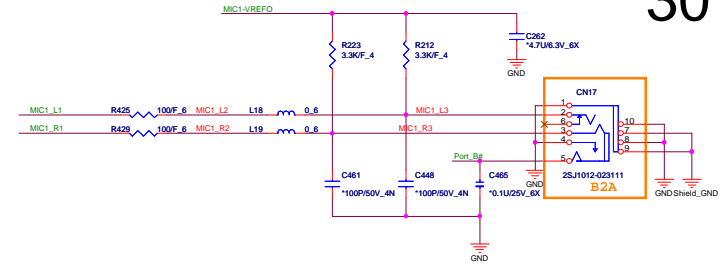
Codec(CX20587-112) <ADO/MDC/AMP>



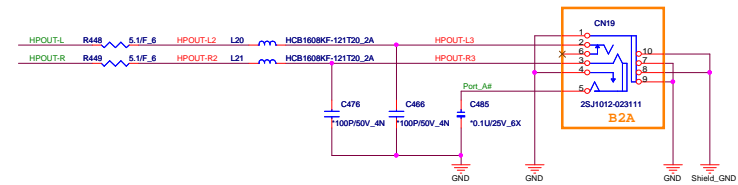
EMI part



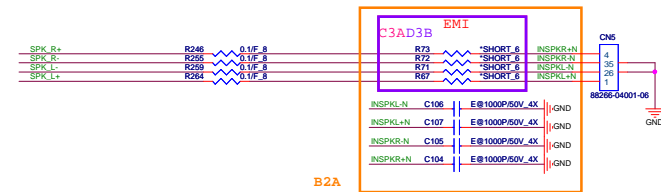
EXT MIC <ADO/AMP>



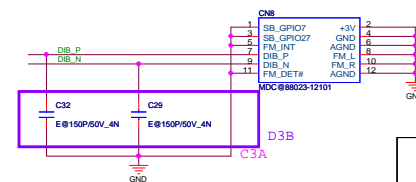
EXT H.P / Beats <ADO/AMP>



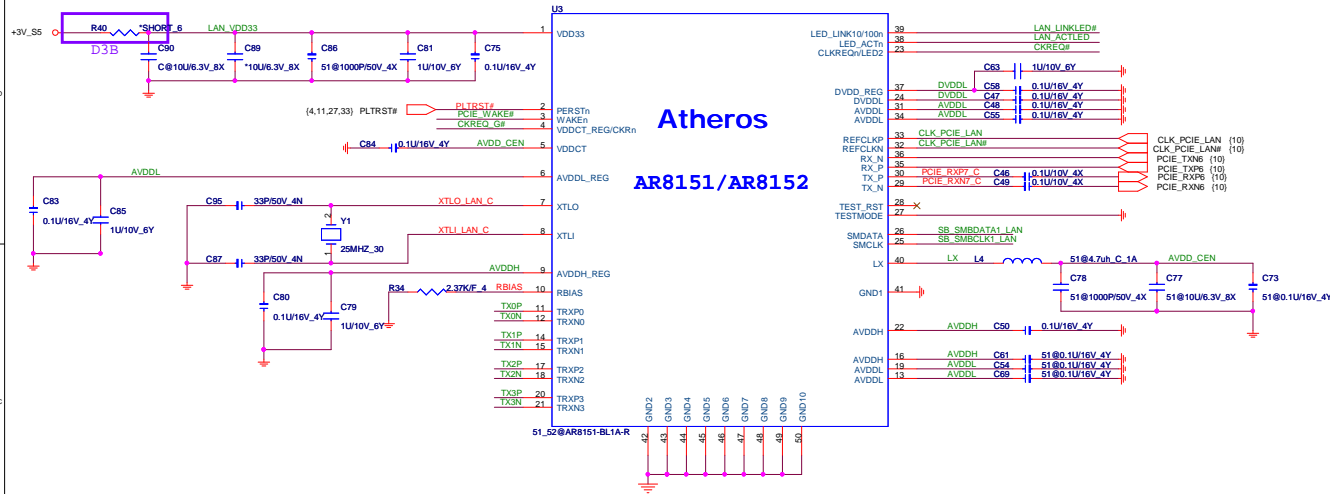
INT SPK <ADO/AMP>



MDC <MDC>



Atheros Lan <LAN/LN1/LNG>



GIGA:AR8151-BL1A-R = AL008151005
10/100:AR8152-BL1A-R = AL008152009

LAN-Wake up function<LAN>

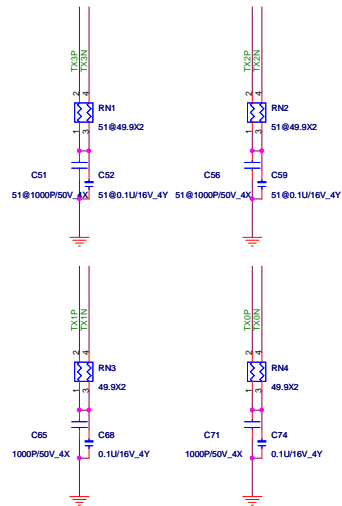
PCIE_WAKE# (11)

LAN-SM-Bus <LAN>

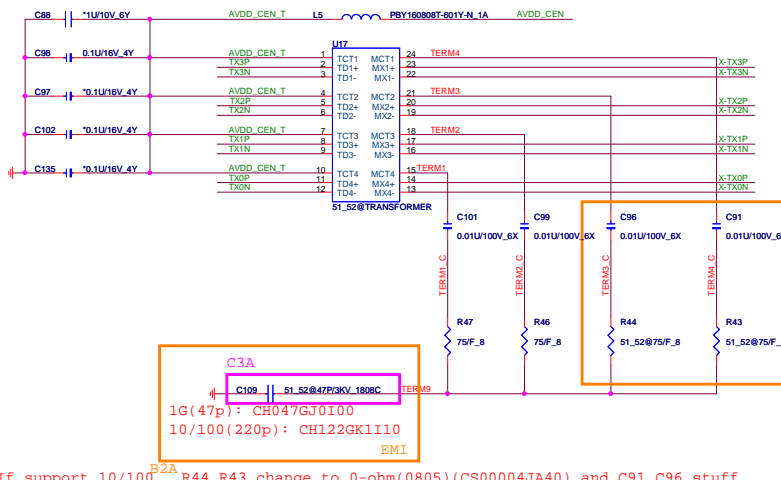
SB_SMBDATA1_LAN R28 0.4 SDA (3,10)
SB_SMBCLK1_LAN R29 0.4 SCL (3,10)

LAN-terminator <LAN/LN1/LNG>

PLACE NEAR LAN IC SIDE



LAN-Transformer <LAN/LN1/LNG>



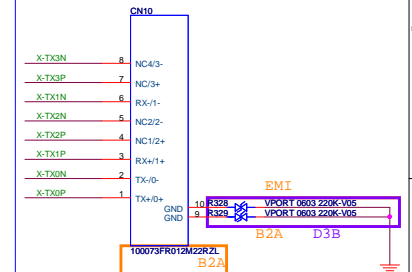
If support 10/100, R44,R43 change to 0-ohm(0805) (CS00004JA40),and C91,C96 stuff
If support 1G, R44,R43 change to 75-ohm(0805) (DS07504FA11),and C91,C96 stuff

LAN-Strap function <LAN/LN1/LNG>



LED0 = LAN_ACTLED	1	Over-clocking enable (default = 1)
	0	Over-clocking disable
LED1 = LAN_LINKLED#	1	SWR switch-mode regulator select Giga LAN pull High (default = 1)
	0	LDO linear regulator select 10/100M LAN pull Low
CKREQ# or CKREQ_G#	1	Normal function
	0	ATE test mode

LAN(RJ45)-CONN Interface <LAN>



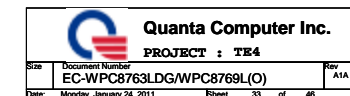
Card reader controller <MMC>



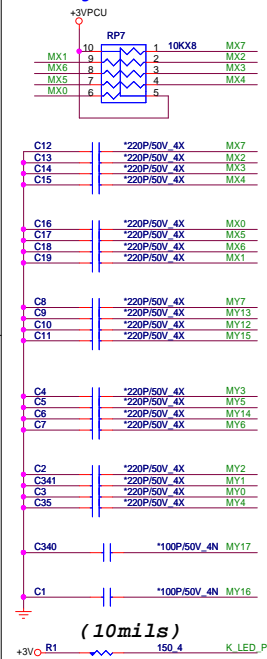
QFN24

<MMC>

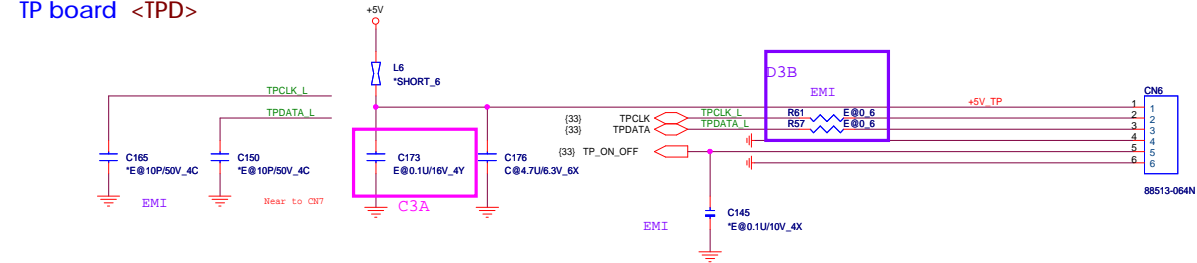




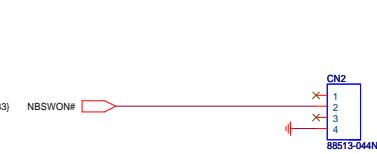
INT KeyBoard <KBC>



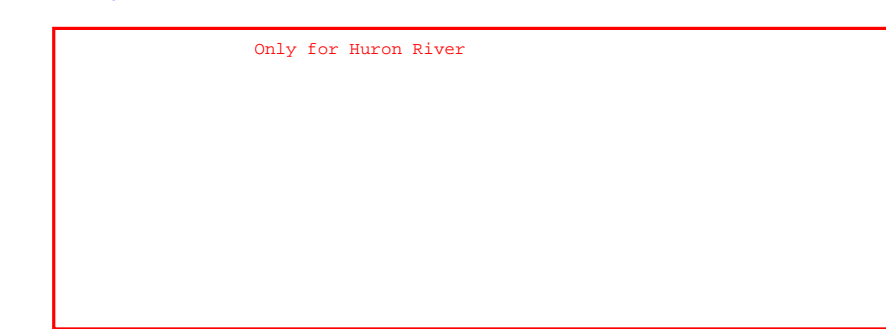
TP board <TPD>



Power board <PSW>

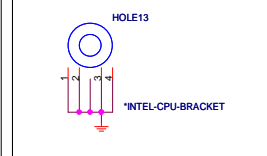


K/B LED power <KBP>

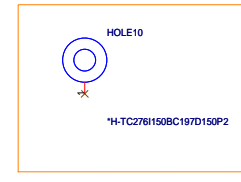
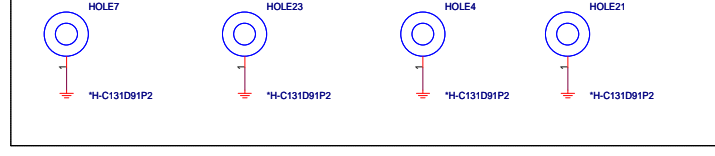


HOLE

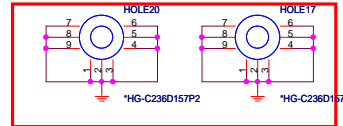
CPU



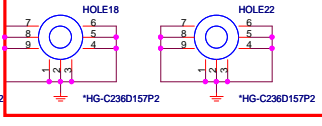
HDD&ODD



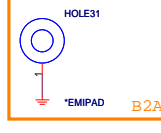
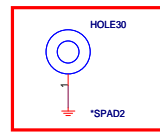
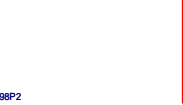
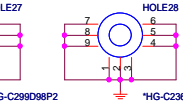
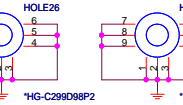
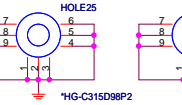
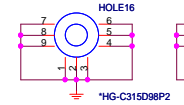
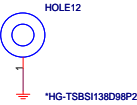
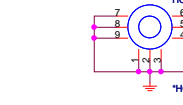
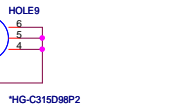
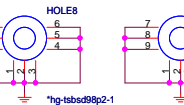
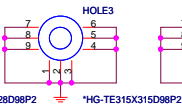
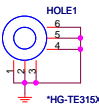
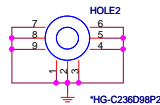
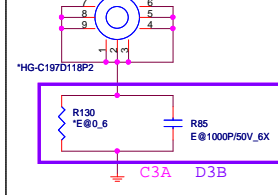
MINI CARD debug Card(上一顆就好)



3G Card(上一顆就好)

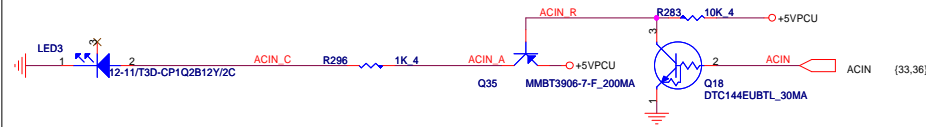


MDC

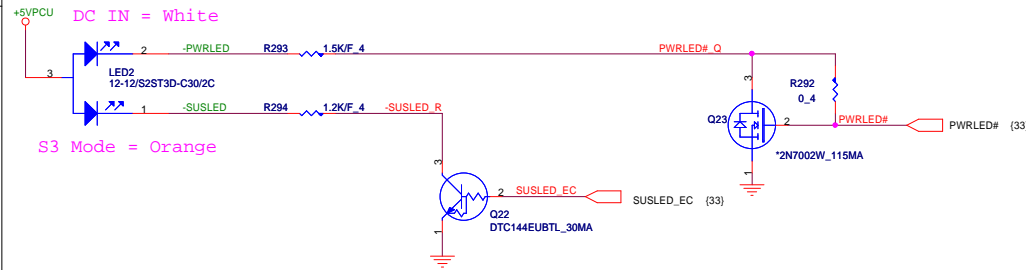


LED

AC-IN



POWER

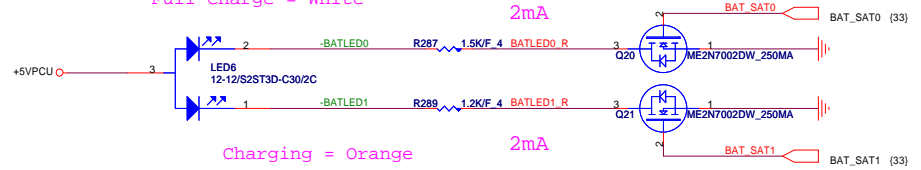


RF LED

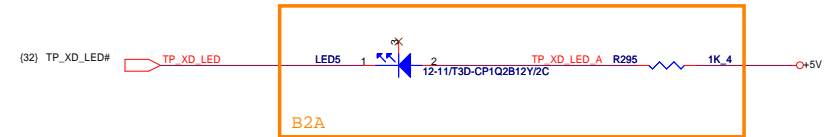


BATTERY

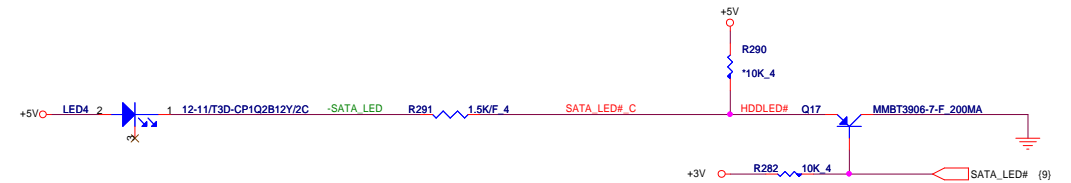
Full Charge = White



CARDREADER

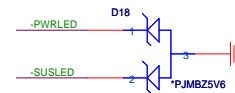


HDD/ODD

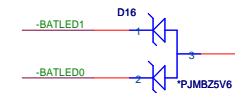


ESD Protect

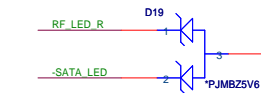
FOR POWER LED



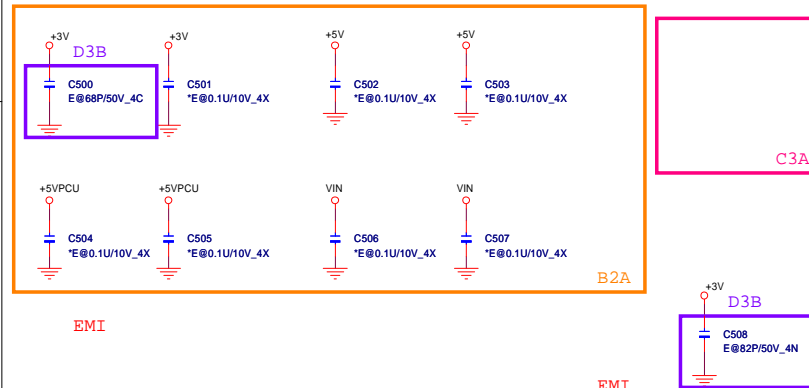
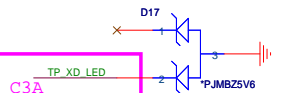
FOR BATTERY LED



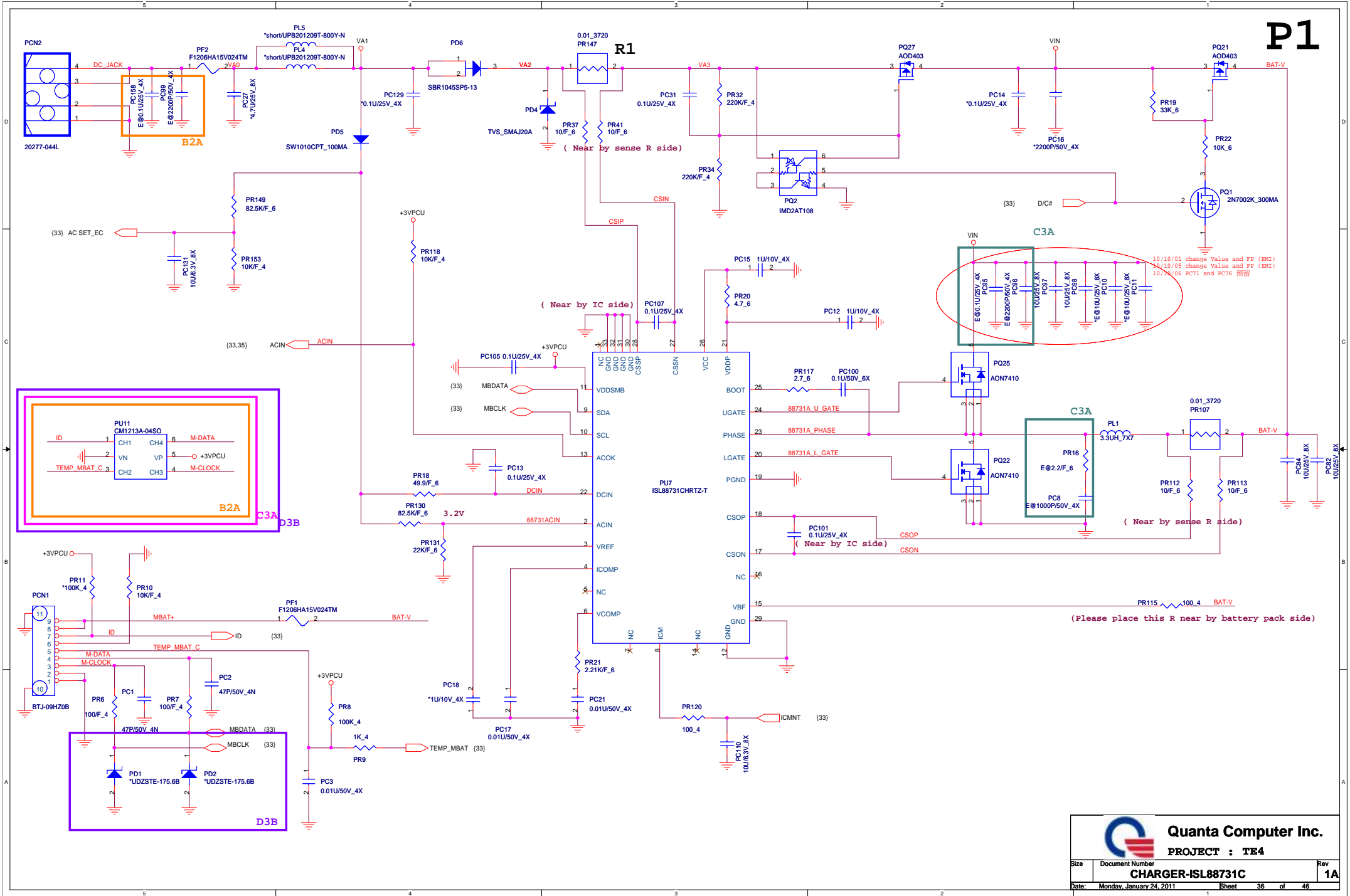
FOR HDD/RF LED



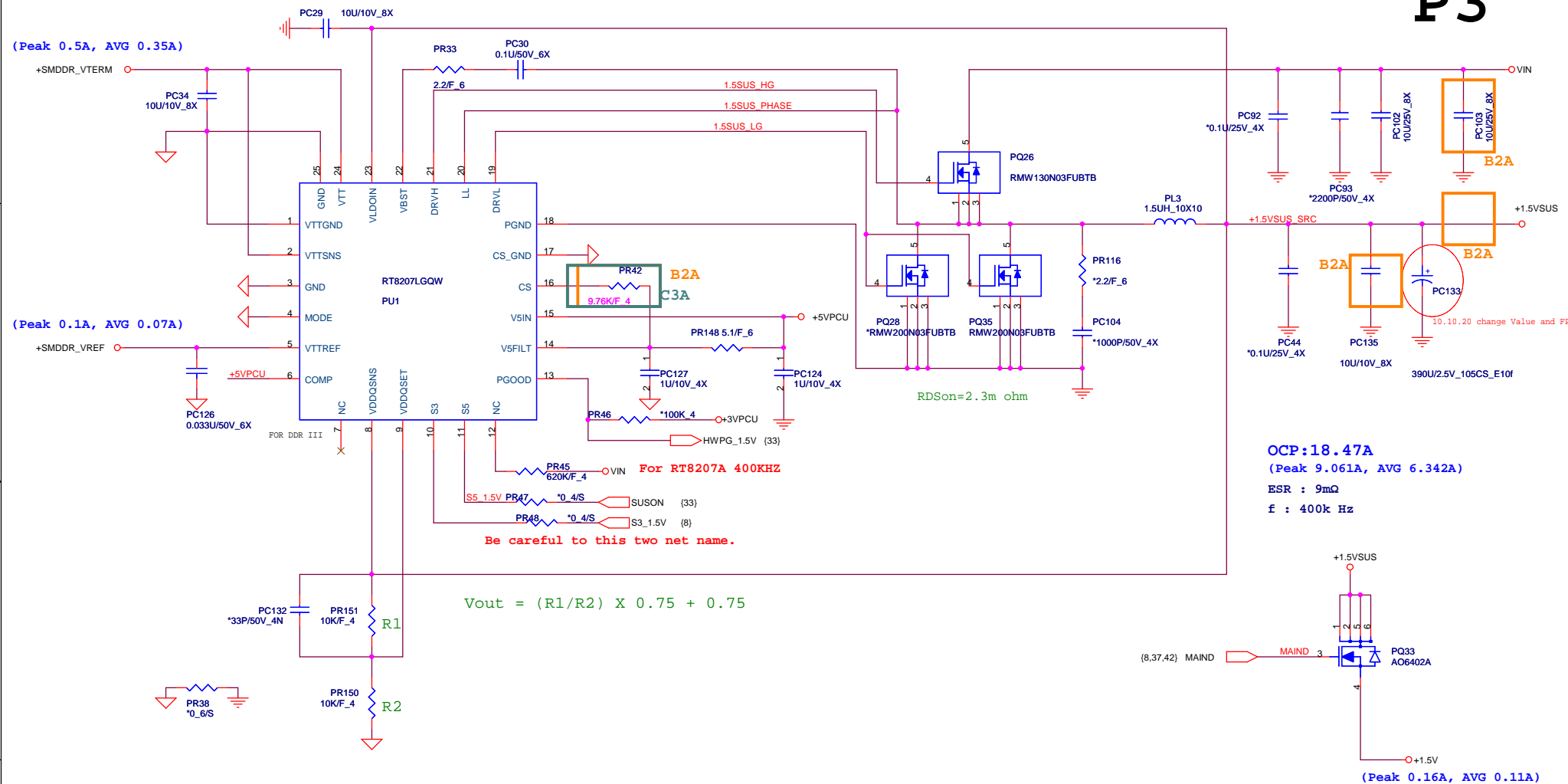
FOR CARDREADER LED



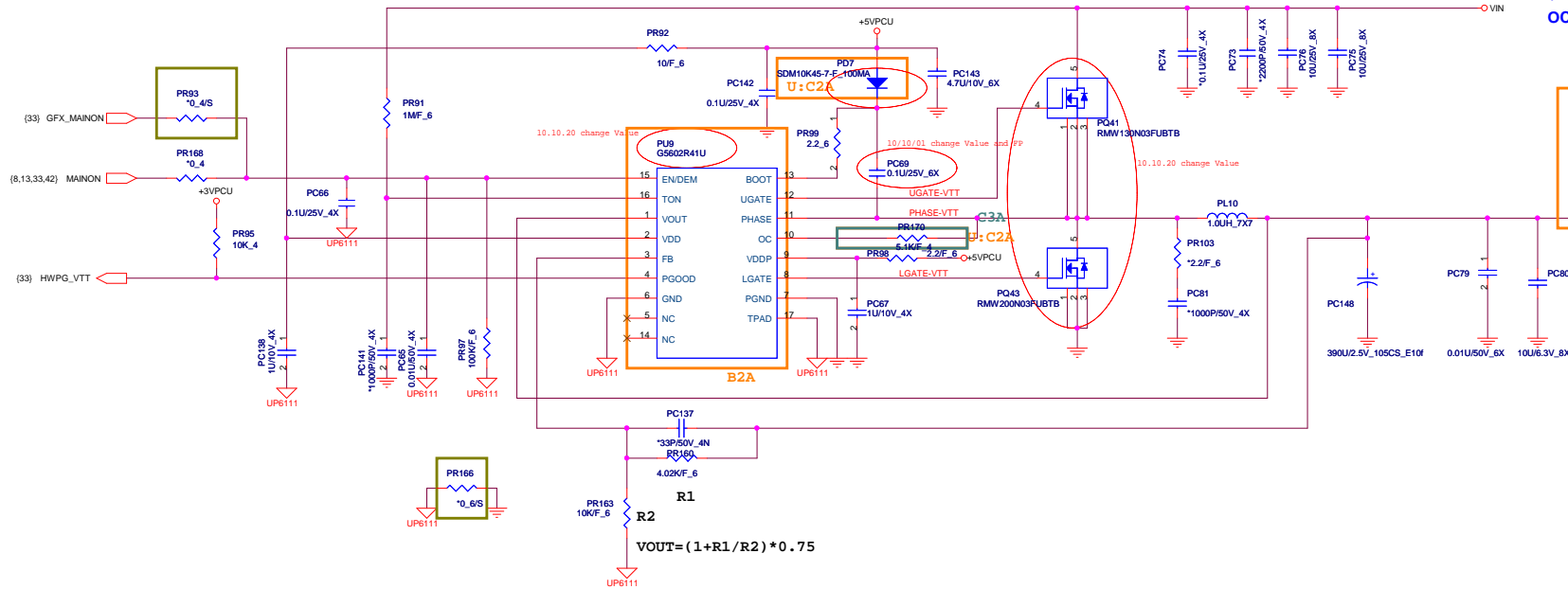
P1




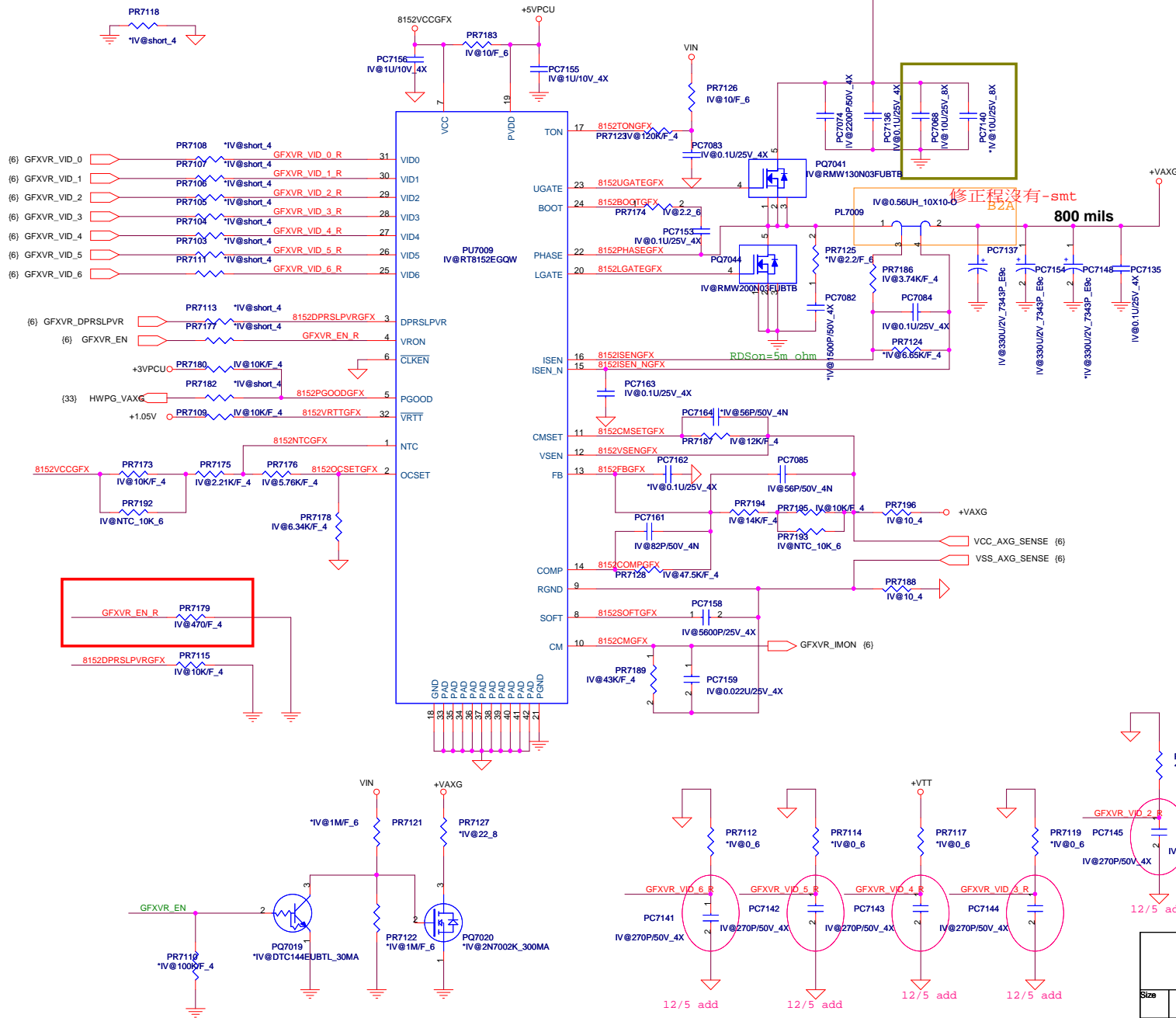
P3



Total capacitor : 390uF
F: 320k Hz
(Peak 24.390A , AVG 17.073A)
OCP:20.104A



 <div> <p>Quanta Computer Inc.</p> <p>PROJECT : TE4</p> </div>		Rev 1A
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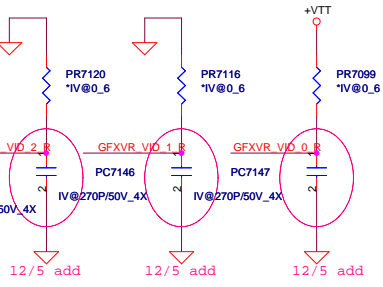


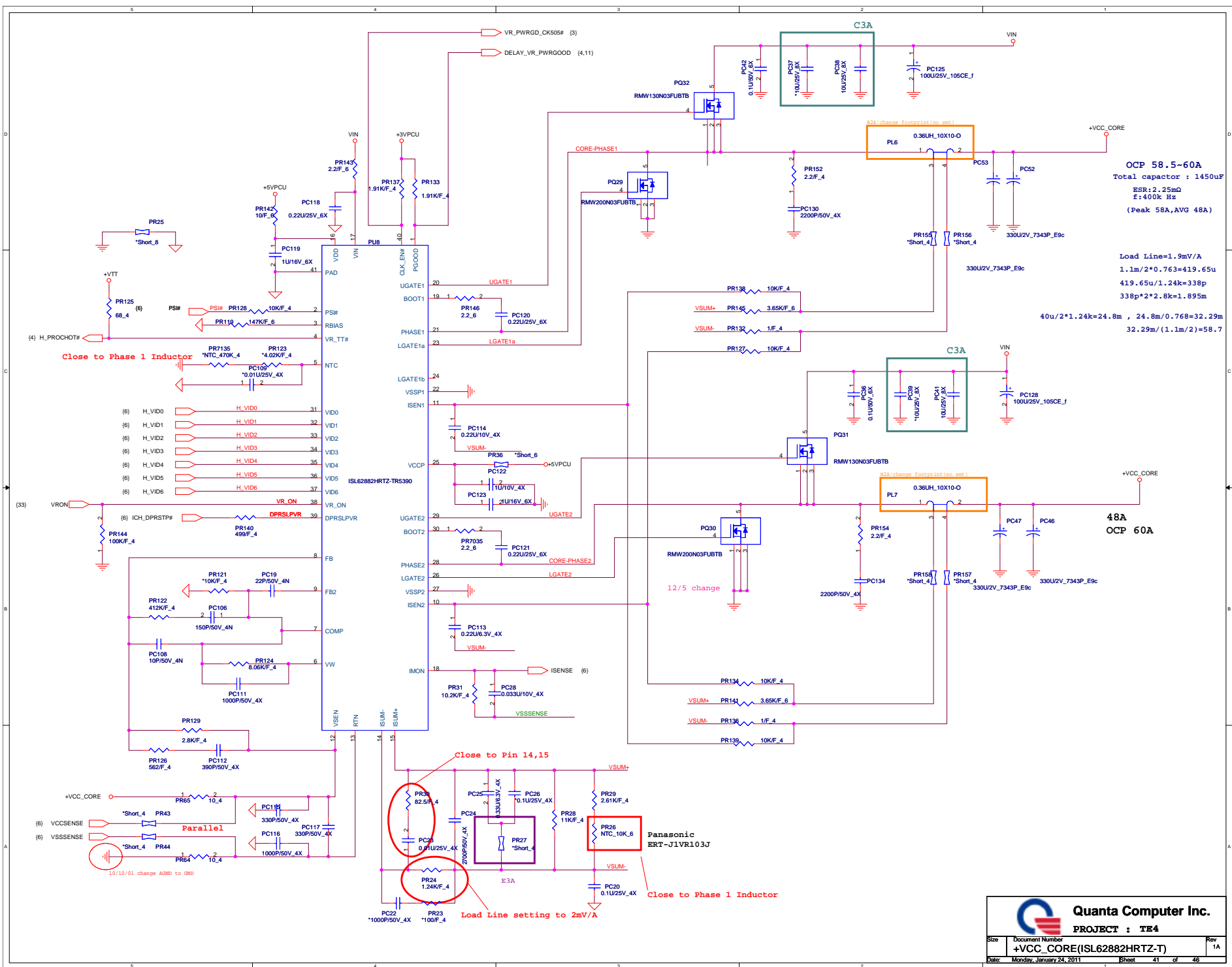
OCF 20A
(Peak 19A, AVG 15.4A)

Total capacitor : 330 uF
ESR : 4.5mQ
f : 300k Hz

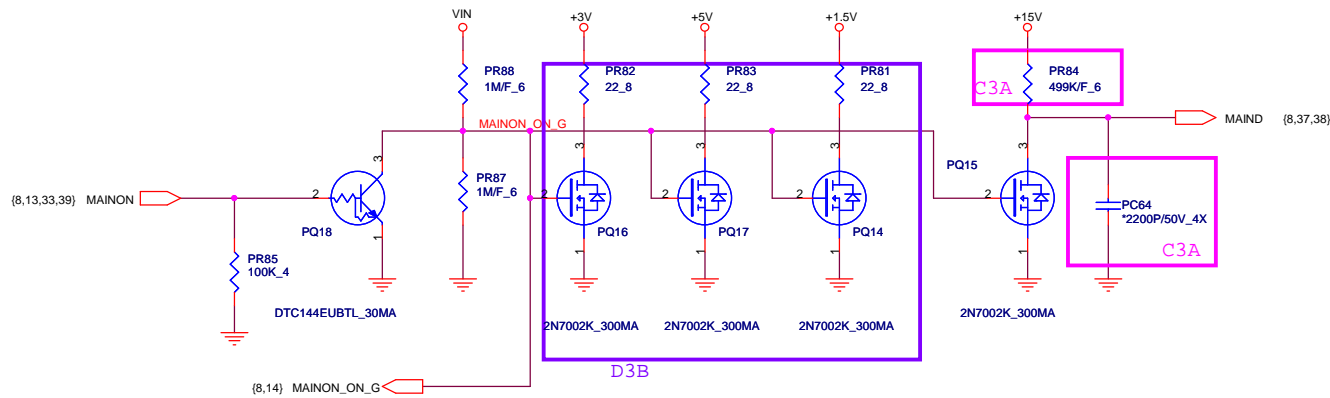
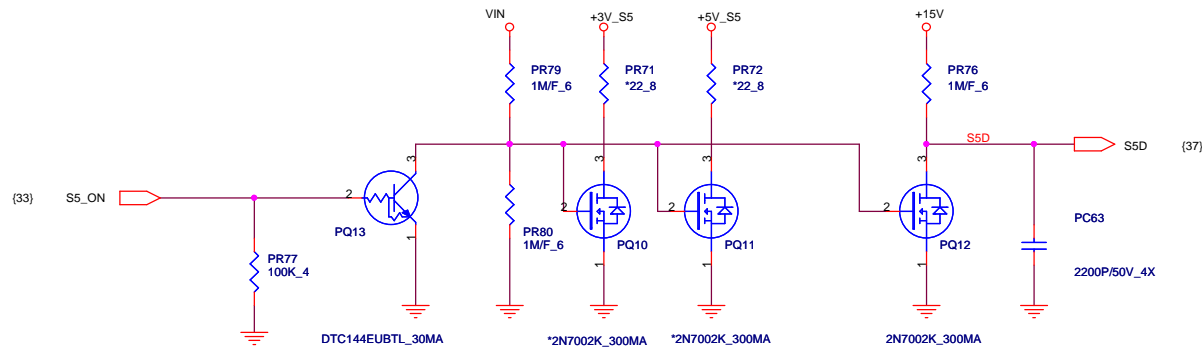
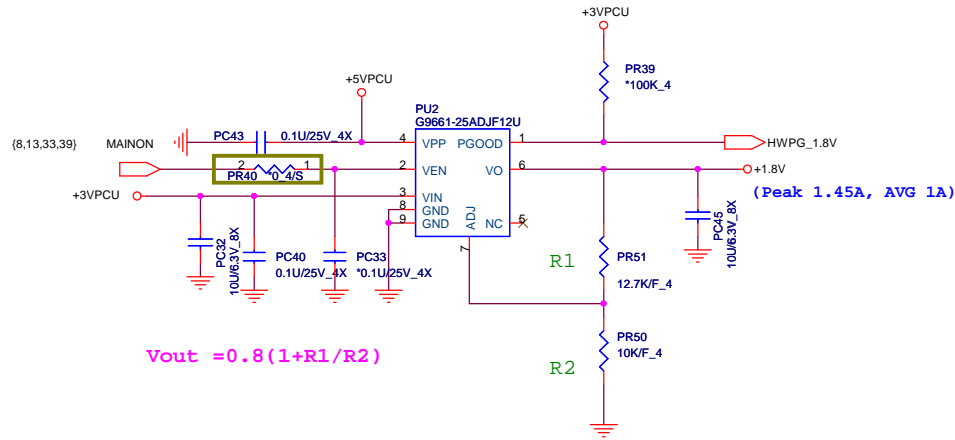
修正程没有-smt
B2A

800 mils



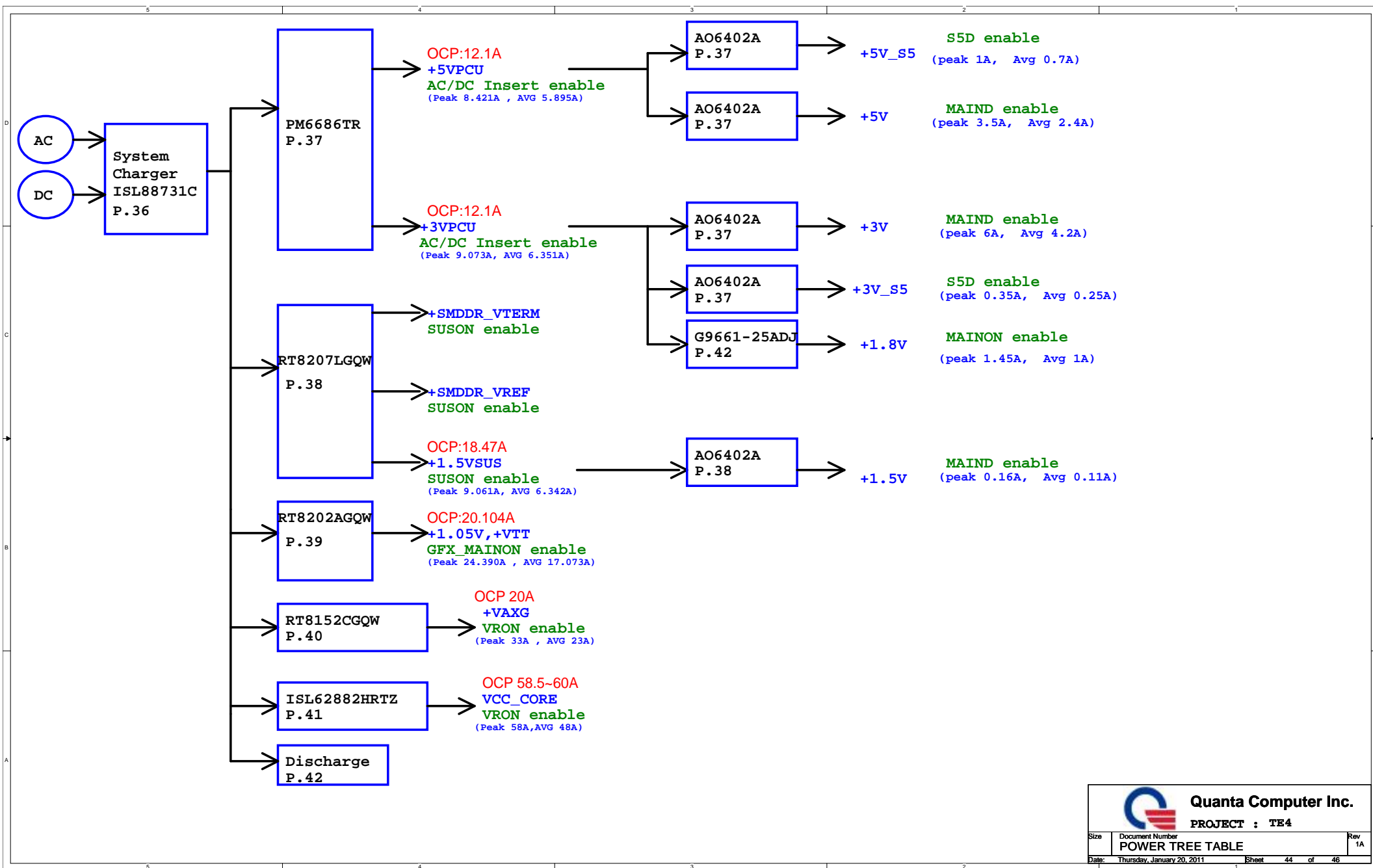


P7



Quanta Computer Inc.
PROJECT : TE4

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	+1.8V (G966A)/Discharge	1A
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[illegible]

